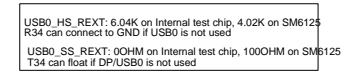

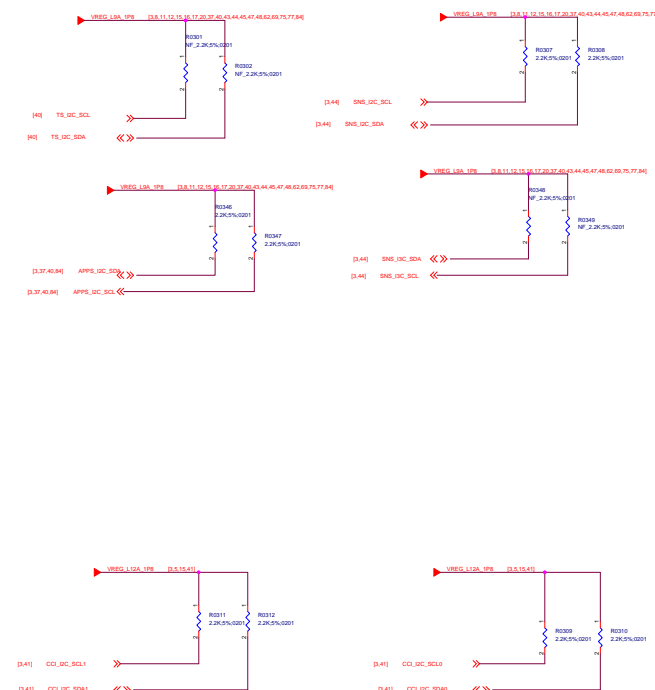


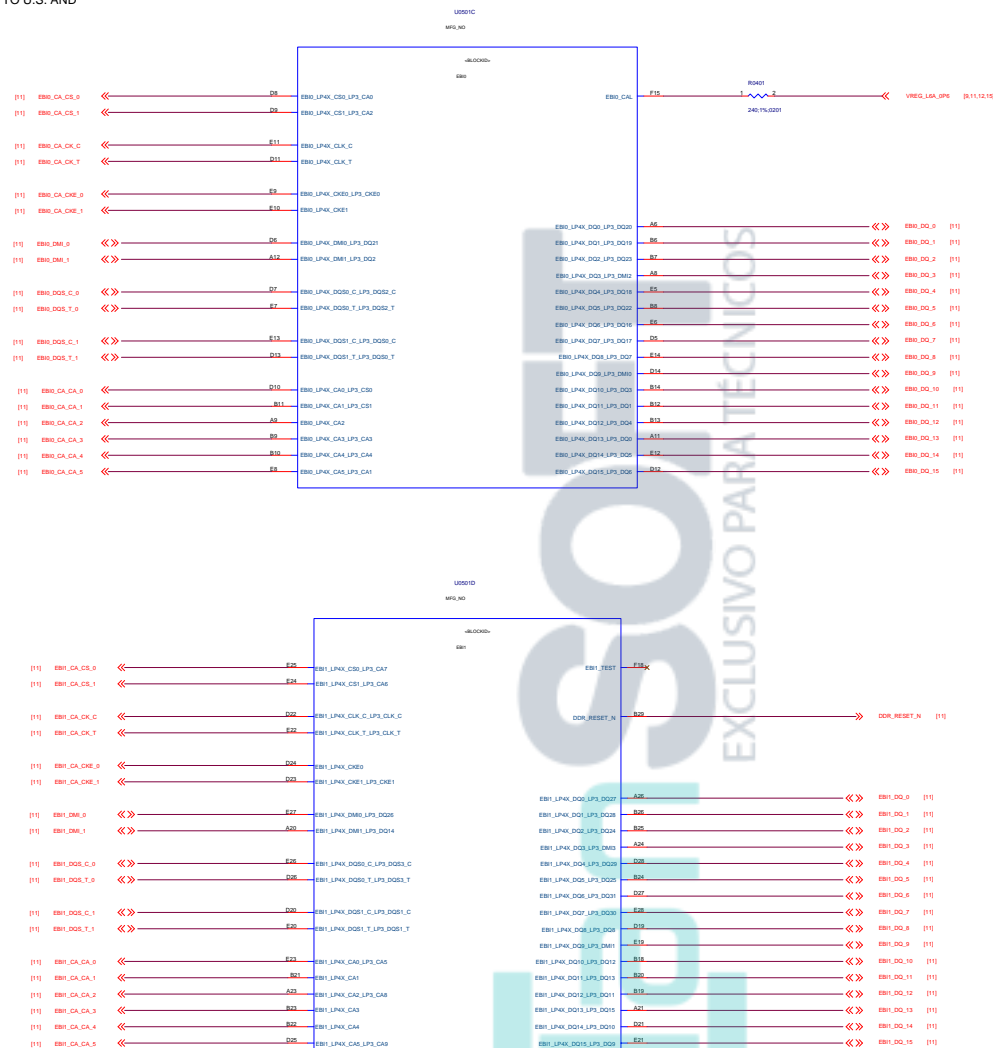
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DOCUMENT NO.:	Design Name = 00718_1_130414_201008041543.katam		
DEPARTMENT:	DESIGN/ENGINEER = shangjiafang		
			
Date:	Page Modify Date = Wednesday, September 8, 2010 2		of 53




Title	Page Name = 03_SM6125 GPO	V10
DOCUMENT NO.:	Design Name = 88718_1_13814_20150425150	
DEPARTMENT:	DESIGNER = shanghe	
		
Date:	Data Month/Date = Wednesday, September 9/2015 3:04:53	



Title	Page Name = 04_SM6125 E000_410		
DOCUMENT NO.:	Design Name = 88718_1_13814_20190808_152bottom		
DEPARTMENT:	DESIGN/ENGINEER = zhangfengjing		
			
Date:	Page Modify Date = Wednesday, September 11, 2019 4 of 53		



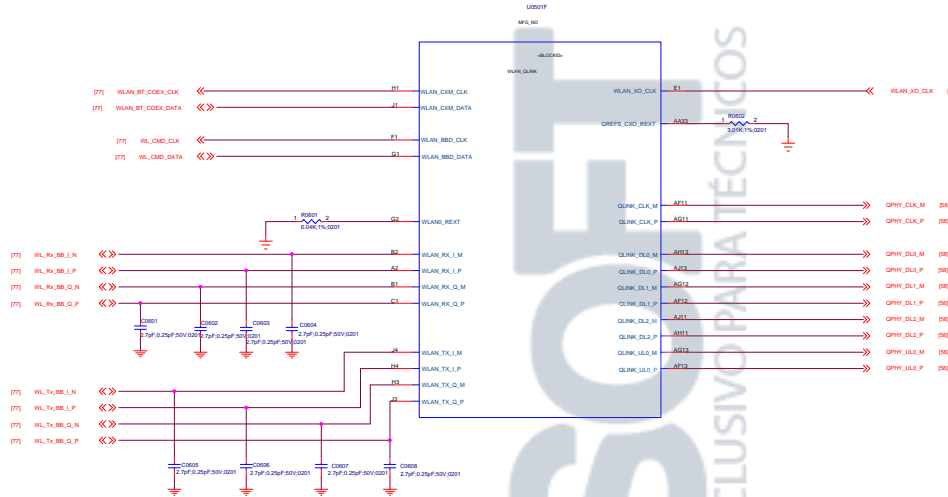
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DOCUMENT NO.:		Design Name = 88718_1_13814_20100228_150Custom	
DEPARTMENT:		DESIGNER/ENGINEER = shangjie	
			
Date: Page Modify Date = Wednesday, September 22, 2015 5 of 53			



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	DESCRIPTION	DATE	APPROVED
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Add C1001-C1008 caps place holder for CLK densense to improve sensitivity.

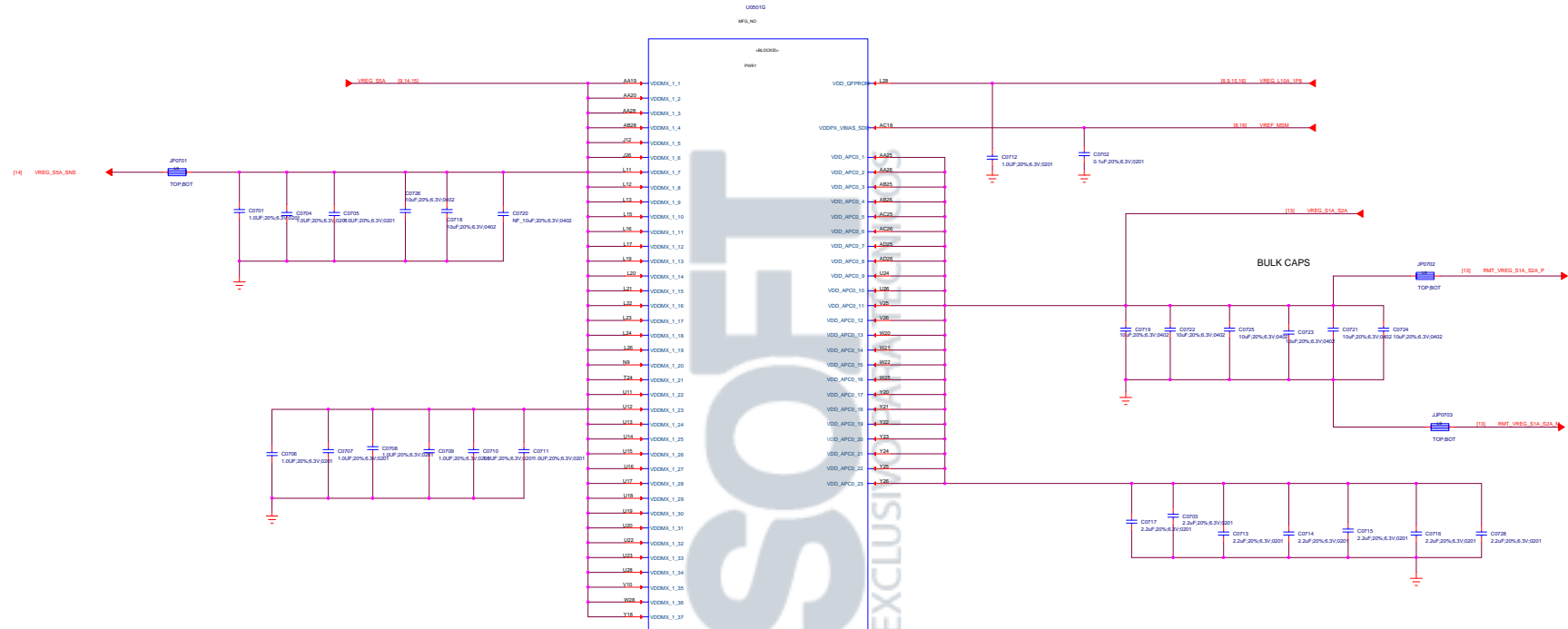
SM6125 WCSS/RF

File Name	Page Name = 06_SM6125 WCSS/RF
Document No.	Design Name = 06718_1_13814_20100808_150000
Department	DESIGN/CMC/ICR - shengsheng
Page No.	Page No. 1 of 1

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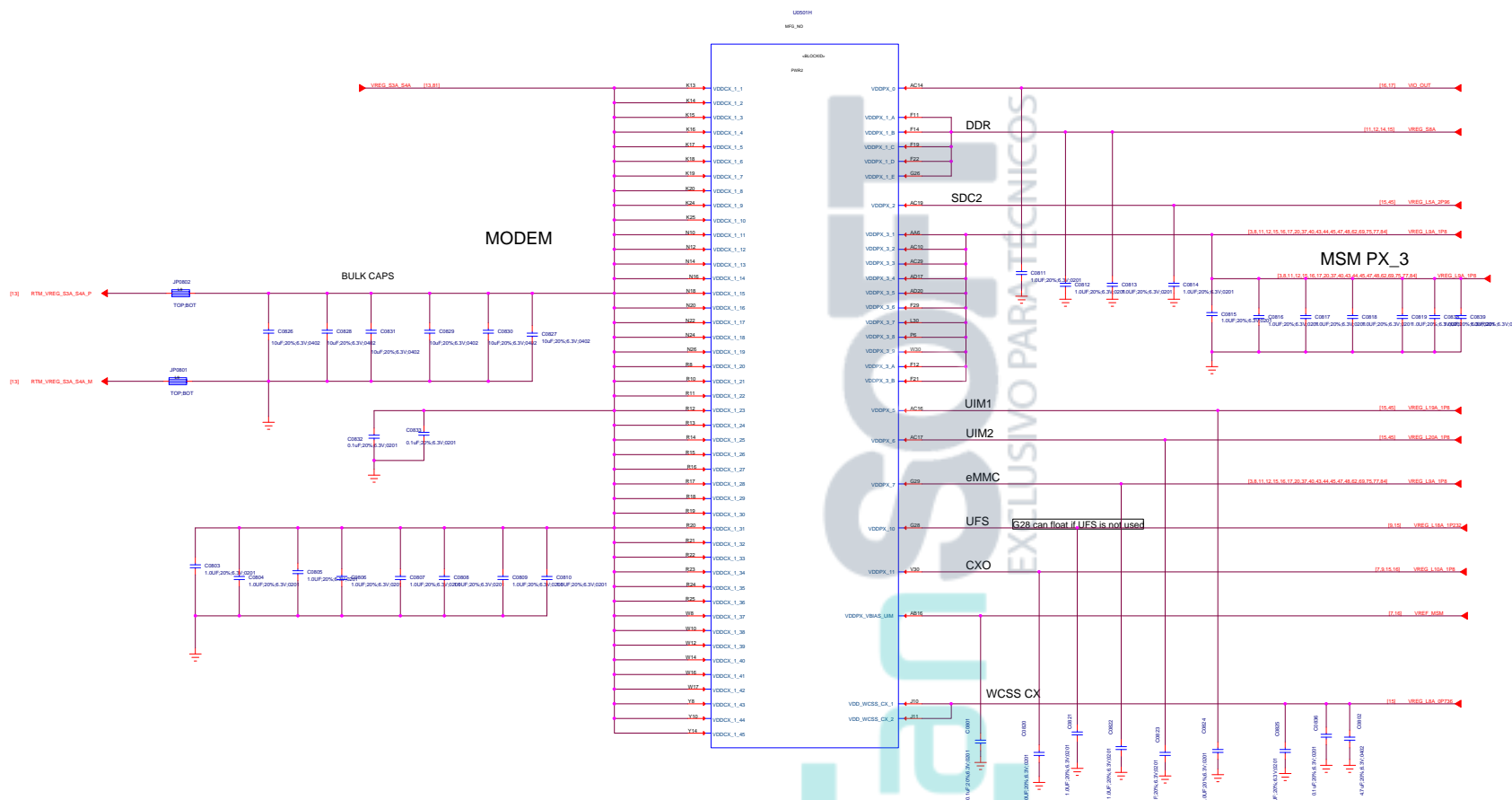
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LTR	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE		



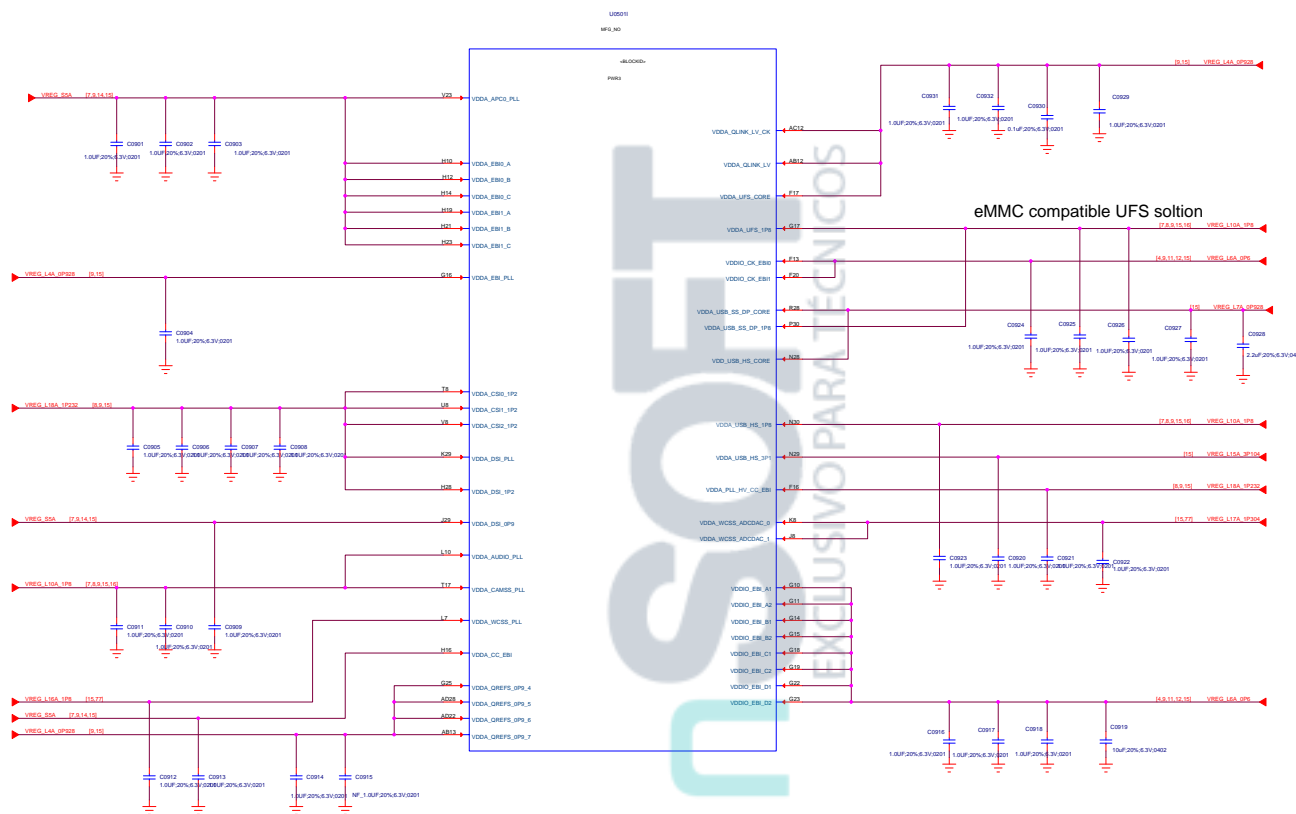
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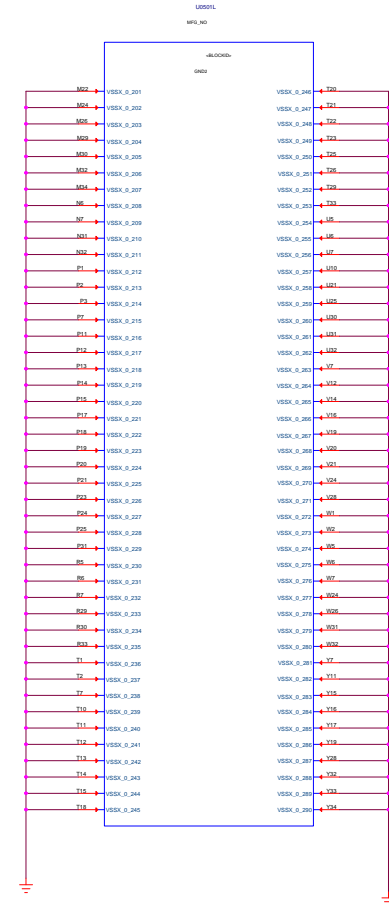
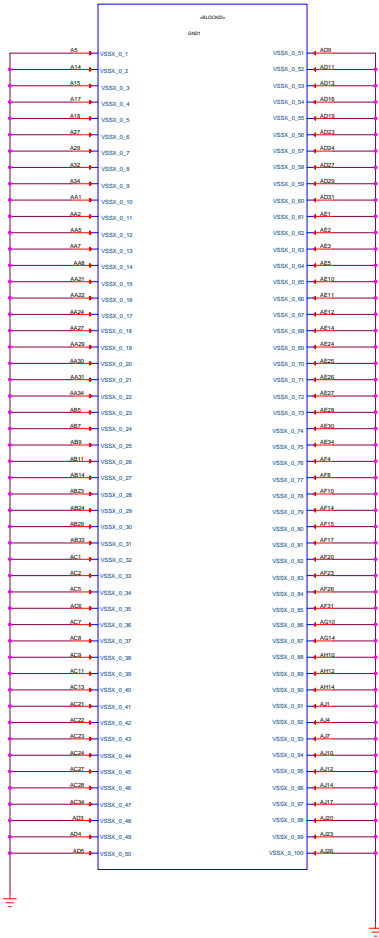


Title	Page Name = 09_SM6125 PUR 3	Page No = 3 of 10
DOCUMENT NO:	Design Name = 08718_1_13M14_20150625	Project Name = 08718
DEPARTMENT:	DESIGNER = xiangling	
		
Date:	Page Modify Date = Wednesday, September 2, 2015	Page 2 of 3



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SM6125 GND

File	Page Name = 10_SM6125 GND	Ver	
DOCUMENT NO.	Design Name = SM6125_1_13M14_20100	Rev	0015
DEPARTMENT	DESIGN/ENGINEERING	Author	chunghyeon
Part	Page Modify Date = Wednesday, Sep 10, 2010	Ver	00

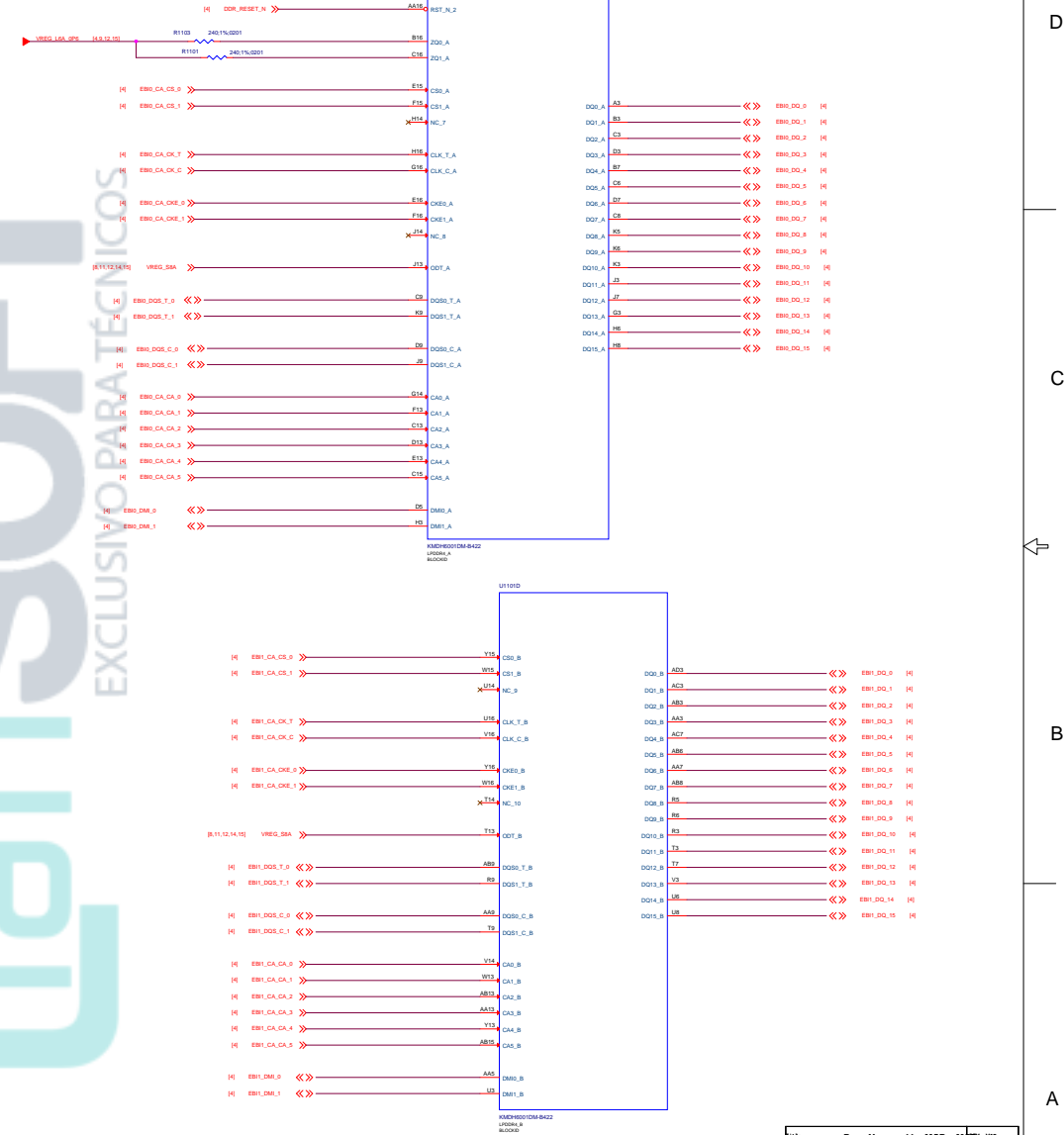
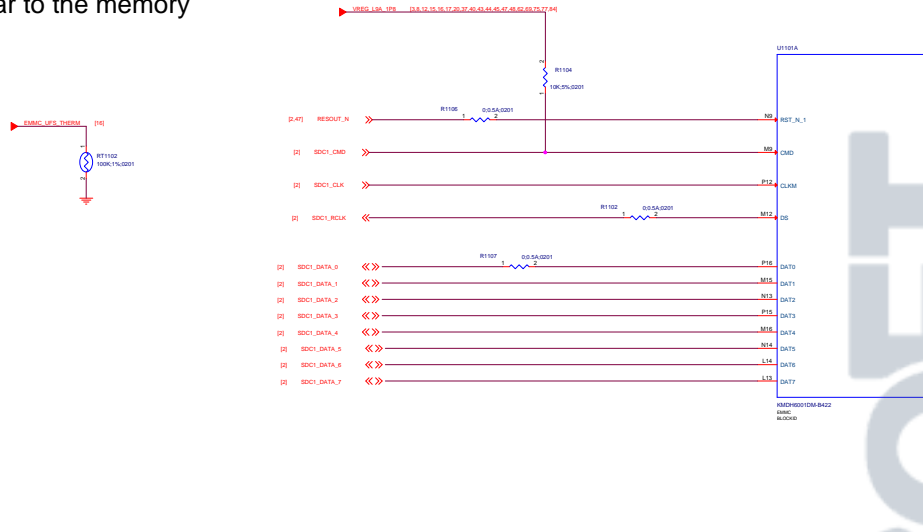
VERSION	1	EDITED BY	LAST_EDITOR	LAST EDIT DATE	2-23-2007_10:06
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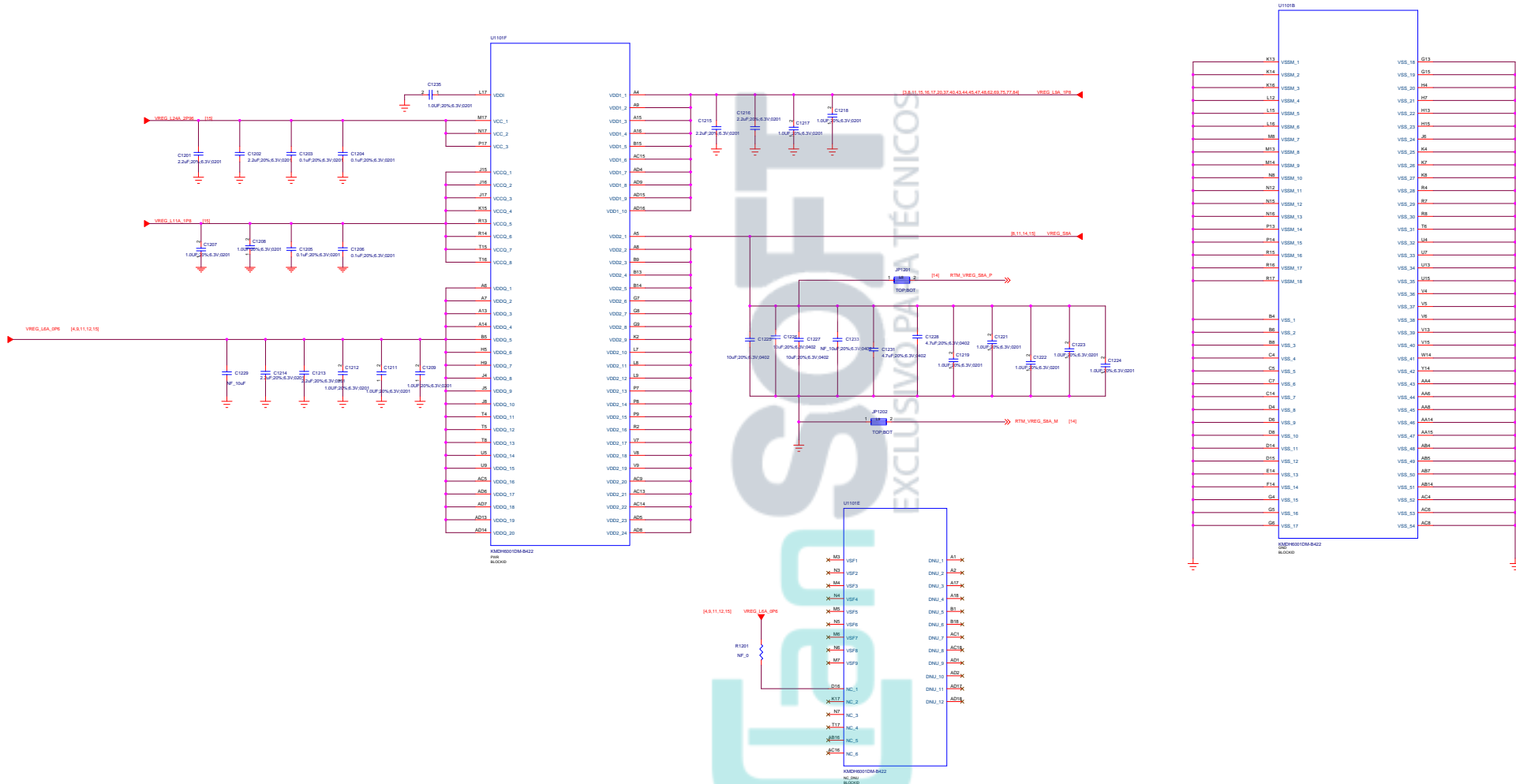
eMCP and DDR4X

Pls near to the memory



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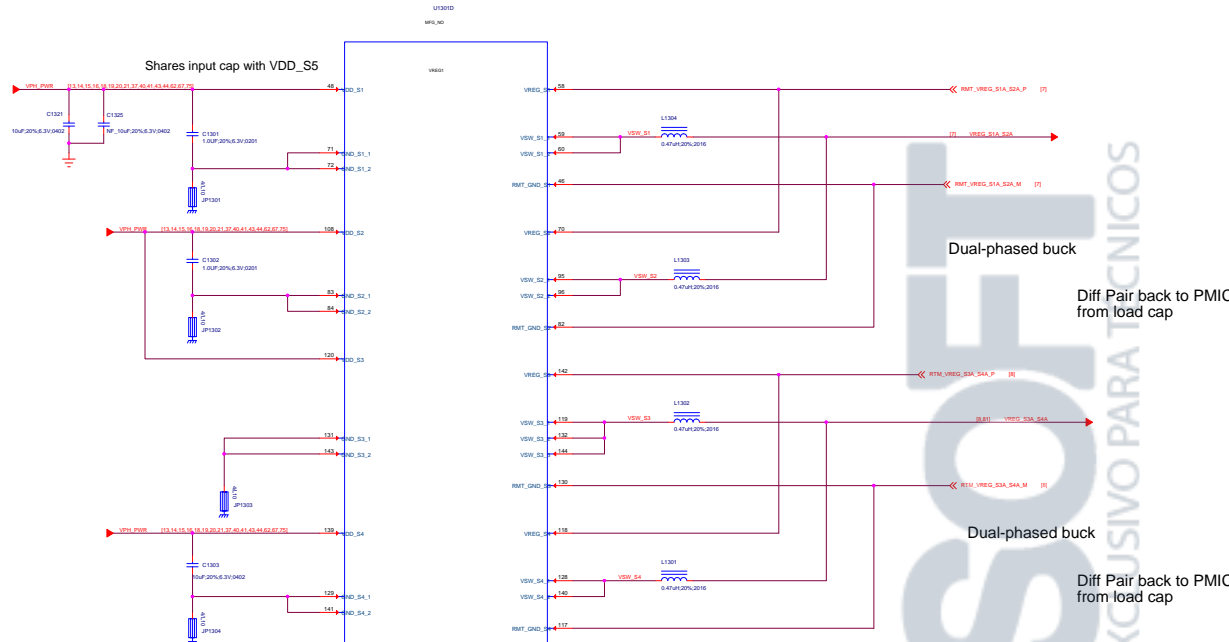
eMCP_POWER

Page Name = 12_EMCP_POWER TM	
DOCUMENT NO. Design Name = 82718_1_13M14_20100904	Rev 04/04/2010
DEPARTMENT: DESIGN/ENGINEERING	DESIGN/ENGINEERING
Qualcomm	
Page: Modify Date = Wednesday, October 14, 2010 12:12 of 53	

VERSION	EDITED BY	LAST EDIT DATE
1	LAST_EDITOR	2-23-2007_10:06

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VREG_S1A is REMOTE diff sense,
VREG_Sx & RMT_GND_Sx should be routed as a differential pair
Do not route VREG_Sx & RMT_GND_Sx near VIN_Sx
Do not route VREG_Sx & RMT_GND_Sx near VSW_Sx unless separated by ground shield

VREG_S2A is REMOTE diff sense,

VREG_Sx & RMT_GND_Sx should be routed as a differential pair
Do not route VREG_Sx & RMT_GND_Sx near VIN_Sx
Do not route VREG_Sx & RMT_GND_Sx near VSW_Sx unless separated by ground shield

VREG_S3A is REMOTE diff sense,
VREG_Sx & RMT_GND_Sx should be routed as a differential pair
Do not route VREG_Sx & RMT_GND_Sx near VIN_Sx
Do not route VREG_Sx & RMT_GND_Sx near VSW_Sx unless separated by ground shield

VREG_S4A is REMOTE diff sense,
VREG_Sx & RMT_GND_Sx should be routed as a differential pair
Do not route VREG_Sx & RMT_GND_Sx near VIN_Sx
Do not route VREG_Sx & RMT_GND_Sx near VSW_Sx unless separated by ground shield

Place Cin as close to PMIC as possible to achieve this requirement.
Loop inductance from (VIN_Sx to Cin + Cin to GND_Sx) must be < 3nH

Nicobar Power Grid v1.31 10/31/2018

S1A-2A:	FTS510	0.8V default	8000mA lpeak	8110.00mA	APC
S3A-4A:	FTS510	0.8V default	8000mA lpeak	8480mA	CX, MODEM
S5A:	HFS510	0.912V default	4000mA lpeak	3620.00mA	EBI, MX, nLDO
S6A:	HFS510	1.352V default	4000mA lpeak	1560mA	LDO
S7A:	HFS510	2.04V default	2500mA lpeak	2350mA	LDO
S8A:	FTS510	1.128V default	4000mA lpeak	1790mA	LDO, LPDDR4x

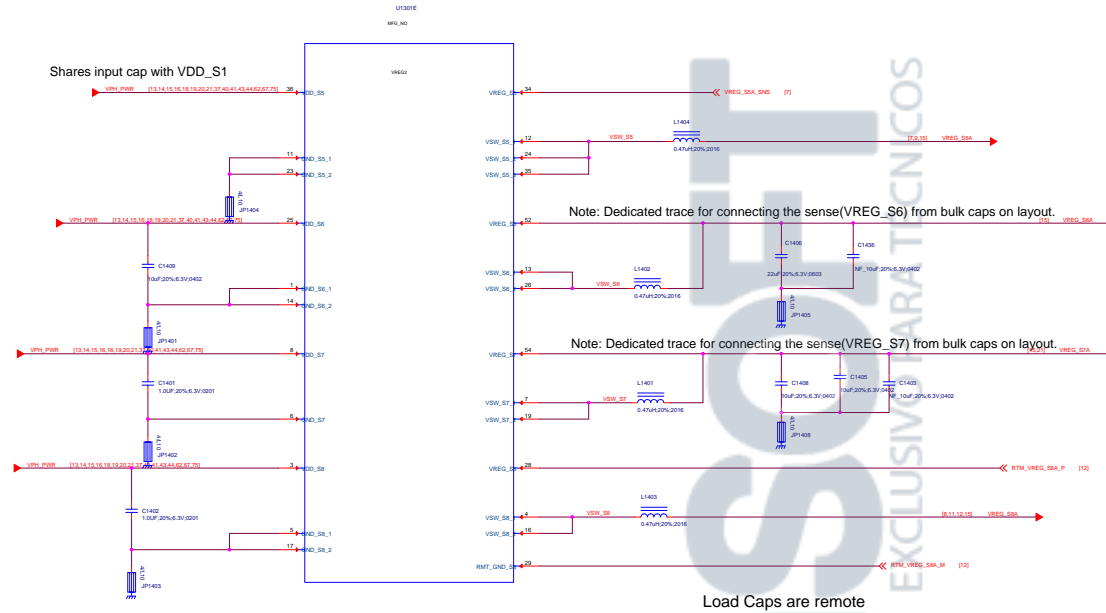
PM6125_Bucks_S1-S4

Page Name = 13_PM6125_Bucks_S1-S4
DOCUMENT NO.: Design Name = MP718_1_130814_20130814_01042013
DEPARTMENT: QUALCOMM/MSB - chipdesign
Date: Page Modify Date = Wednesday, September 26, 2013 13 of 53

VERSION	EDITED BY	LAST EDIT DATE
1	LAST_EDITOR	2-23-2007_10:06

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Place Cin as close to PMIC as possible to achieve this requirement.

Loop inductance from (VIN_Sx to Cin + Cin to GND_Sx) must be < 3nH

Route diff pair out from Cap back to appropriate pins at PMIC

VREG_S8A is LOCAL diff sense,
VREG_Sx & RMT_GND_Sx should be routed as a differential pair
Do not route VREG_Sx & RMT_GND_Sx near VIN_Sx
Do not route VREG_Sx & RMT_GND_Sx near VSW_Sx unless separated by ground shield

PM6125_Bucks_S5-S8

Title		Page Name = 14_PM6125_Bucks_S5-S8	
DOCUMENT NO.		Design Name = 88718_1_13M14_20100	Rev = 1.0
DEPARTMENT		DESIGN/ENGINEERING	
DATE		Page Modify Date = Wednesday, Sep 23, 2008 10:06:10	of 13

VERSION	1	EDITED BY	LAST_EDITOR	LAST EDIT DATE	2-23-2007_10:06
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LDO Input Rail
VDD_L1_L7_L17_L18
VDD_L2_L3_L4
VDD_L5_L15_L19_L20_L21_L22
VDD_L6_L8
VDD_L9_L11
VDD_L10_L13_L14
VDD_L12_L16
VDD_L23_L24

Parent Buck
VREG_S6
VREG_S8
Ext Boost Byp
VREG_S5
VREG_S7
VREG_S7
VREG_S7
Ext Boost Byp

Max Current
1.13
0.816
1.38
0.906
1.01
1.08
0.270
1.161

REV	REVISIONS		DATE	APPROVED
	DESCRIPTION	INITIAL RELEASE		

D

D

C

C

Note: Place LDO input caps near to PMIC

Nicobar Power Grid v1.31 11/12/2018

LDO Type Source V_default (est) Target Pin#
L1 N600 S6A 1.2V (625) QLN,SDR 1.2 61
L2 N300 S8A 1V (320) SDR VDD 1.0V 63
L3 N600 S8A 1V (370) SDR VDD 1.0V 64
L4 N300 S8A 0.928V (126) QLINK, EBI, MIPI 39
L5 MVP50 VPH 2.96V (22) PX 113
L6 N1200 S5A 0.624V (1040) VDDQ, EBI 9
L7 N600 S6A 0.928V (54.2) USB 49
L8 N300 S5A 0.664V (81) CX 33
L9 LVP600 S7A 1.8V (754) Sensors, WCD, TMD, PMI_MSM, QET 43
L10 LVP150 S7A 1.8V (100) QFPROM, USB,UFS, PX 81
L11 LVP600 S7A 1.8V (925) EMMC/VCCQ 45
L12 LVP300 S7A 1.8V (121) OV, USB, REDRIVER 69
L13 LVP300 S7A 1.8V (204) QPM 1.8V, BBRX, GPS 105
L14 LVP600 S7A 1.8V (650) WCD Buck 94,93
L15 MVP150 VPH 3.128V (5.28) USB 3.1V, DP PHY 114
L16 LVP150 S7A 1.8V (92.5) WCSS, WCN_XO 93
L17 N300 S6A 1.304V (246) WCN, WCSS ADX DAC 38
L18 N300 S6A 1.232V (133) MIPI, VDDPX 37
L19 MVP150 VPH/BB 1.8V (60.2) Memory, SN100, PX 126
L20 MVP150 VPH/BB 1.8V (60.2) Memory, SN100, PX 138
L21 MVP600 VPH/BB 2.704V (0.68) QAT, DFE, RTC, QSW 136
L22 MVP600 VPH/BB 2.96V (800) MMC 137
L23 MVP600 VPH/BB 3.304V (591) WCN 3.3V 41
L24 MVP600 VPH/BB 2.96V (1170) EMMC 31

PM6125_LDOs

LDO L5/L9/L10/L11/L12/L13/L14/L15/L16/L19/L20/L21/L22/L23/L24 is the Pseudo-capless LDO, so can dni CAP in BOM
PSEUDO CAPLESS LDOs
P-type are psuedo-capless, cap can be at load
For CAPLESS LDOs: If decaps on the load side do not add up to LDO spec, then install the cap close to the PMIC

1.0uF

2.2uF

A

1114	Page Name = 15_PM6125_LDOs	1110
DOCUMENT NO.	Design Name = 88714_1_13M14_20180808	1110
DEPARTMENT:	DESIGN/ENGINEERING	
Rev:	Page Modify Date = Wednesday, September 13, 2018	11

VERSION

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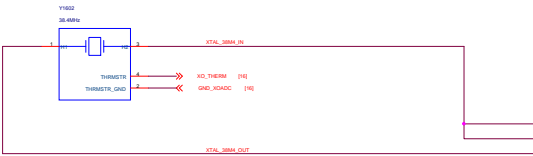
Layout Note:
No trace shall be present in at-least two immediate layers below XTAL.

Route XTAL IN/OUT trace with
length between 3mm and 10mm

AVDD_BYP should be routed
away from noisy traces

Trace from pin to cap and ONE dedicated via from cap to main ground plane.
DCR < 200mOhm and ESL < 10nH
Do NOT connect to any other ground.

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LTR	DESCRIPTION	DATE
A	INITIAL RELEASE	



If USB the LPDDR3 need this VREF voltage, LPDDR4 don't need it.

TEST_EN_VPP must be grounded in all chipset level
and customer-facing HW schematics.

If RTC support is not needed when the battery is removed, a backup capacitor can be used on the VCOIN pin.
A ceramic capacitor with an effective capacitance of 10uF can support SMPL for up to 1 second.

If you use embedded battery, can remove these capacitors

Critical Layout Guidelines for VREF_RF (go/PmicLayoutChecklist)

Preferred: Short, dedicated route to VREF_RF cap,
away from noisy signals and dedicated via to main ground plane at cap or PMIC pin.

Acceptable: Dedicated via directly to main ground plane at the GND_CLKSXO pin
and at VREF_RF cap (without routing to cap).

Do NOT connect to any other ground.

Loop DCR must be <1000 mΩ.
Loop inductance must be <3 nH.

Placement/Layout Note:
VREG_RF Cap should be placed close to the PMIC
Can be prioritized over VREG_XO Cap placement
Short dedicated route to VREG_RF/XO cap
Dedicated via directly to main ground plane at the capacitor

Dedicated trace from REF_GND to cap.
Dedicated via to main ground plane right under PMIC pin (REF_GND)
or as close to the pin as possible.
Do NOT use a via for cap.
Do NOT use a via for cap.
SPMI_CLK & SPMI_DATA should be routed away from noisy traces
Route signals as a diff pair as much as possible

GND_XOADC
Skinny trace to XTAL components ground.
One dedicated via to main ground plane as close to PMIC pin as possible

Critical Layout Guidelines for Clocks (go/PmicLayoutChecklist)
Coupling to any RFCLK or LNBCLK output from each aggressor should be < 50 fF.
1. SMPS components (Buck, Boost, Charger)
2. VSW_Sx traces (Buck, Boost, Charger)
3. All other RFCLK, LNBCLK
4. Any high speed digital signal
5. Any other noisy signals

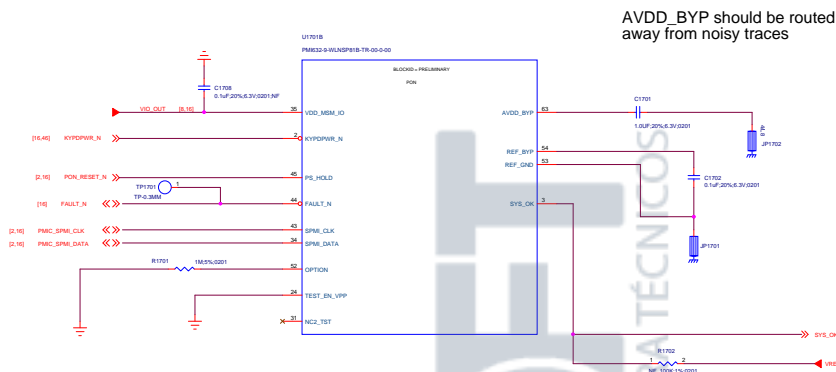
PM6125_HK/IO

Page Name	16_PM6125_HK/IO
Document No.	Design Name = 88718_1_13814_2018080101540
Department	DESIGN/ENGINEERING - smartphone
Date	Page Modify Date = Wednesday, September 19, 2018 16 of 53

VERSION	1	EDITED BY	LAST_EDITOR	LAST EDIT DATE	2-23-2007_10:06
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LTR	DESCRIPTION	DATE	APPROVED
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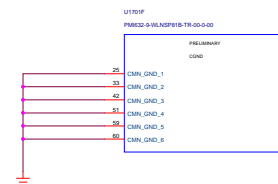
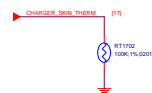
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2	SPML, Micro USB, FMB_EN	R = (33K, 3.9K, 4.7K, and 5.6K)
3	I2C, Micro USB, FMB_DIS	R = (8.2k, 10k, 12k, 15k)
4	I2C, Micro USB, FMB_EN	R = (22k, 27k, 33k, and 39k)
5	I2C, Type-C, FMB_DIS	R = (56k, 68k, 82k, and 100k)
6	I2C, Type-C, FMB_EN	R = (150k, 180k, and 220k)
7	SPML, Type-C, FMB_DIS	R = (330k, 390k, and 470k)
8	SPML, Type-C, FMB_EN	R = (820k, 1M, 1.2M, and Open)



Trace from pin to cap and ONE dedicated via from cap to main ground plane.
DCR < 200mOhm and ESL < 10nH
Do NOT connect to any other ground.

Dedicated trace from REF_BYP to cap.
Dedicated trace from REF_GND to cap.
Dedicated via to main ground plane right under PMIC pin (REF_GND)
or as close to the pin as possible.
Do NOT add via at cap.

REF_BYP and REF_GND should be
routed away from noisy traces



GPIO#	GPIO Function
GPIO1 (LV)	FMB1 (Output mode) / TypeC_CONN_THERM_SNS / MSM/eMMC THERM
GPIO2 (MV)	SMB_EN / H/LED / (SINK required ?Fixed 10mA)
GPIO3_AMUX	Skin_Therm_Sns / FLASH_THERM_SNS
GPIO4 (LV)	I2C_IRQ (Output) / TypeC_CONN_THERM_SNS / FMB2 (Output)
GPIO5_AMUX (MV)	SMB_THERM_SNS / Flash_Strobe / USB_ID
GPIO6 (LV)	WLED_EN
GPIO7_AMUX (LV)	SMB_VCHG_P
GPIO8_AMUX (LV)	FMB2 (Output) / SMB_VHG_M

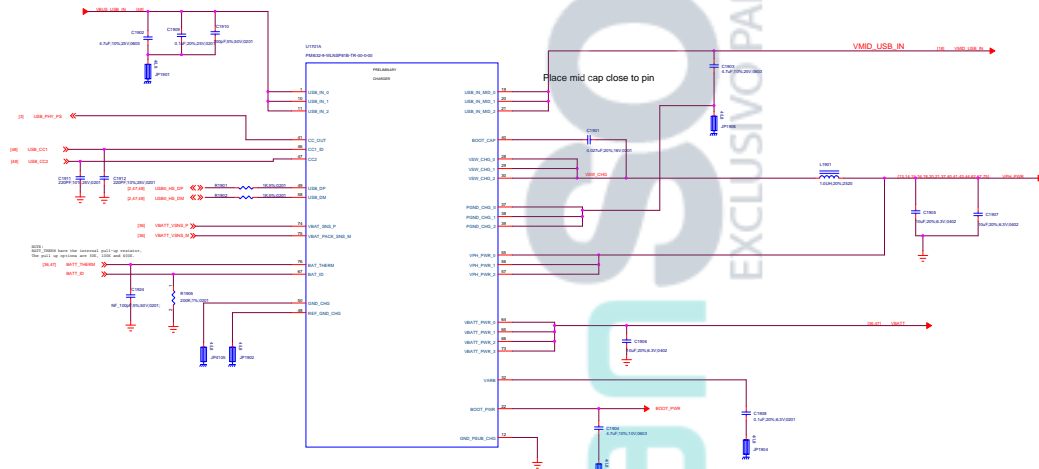
PMI632_Control

Title		Page Name = 17_PMI632_CONTROL	
DOCUMENT NO.:		Design Name = 86718_1_13M14_2015041501.dwg	
DEPARTMENT:		DESIGN/OWNER = shangqiang	
RYINGTECH			
Date: Page Month/Date = Wednesday, September 20, 2019 17 of 53			

NOTE:
C1902 can use the 25V capacitor too,
just for the BOM category normalized

NOTE:
recommand to use battery NTC values 100K, B=4250
Layout Note:
PACK_SNS_M should have a dedicated route to
battery connector negative sense

NOTE:
Use C1902= 2.2uF for parallel Charging Config
Use C1902= 4.7uF for only PMI Charging Config



CAD NOTE:
Dedicated VIA to Main GND

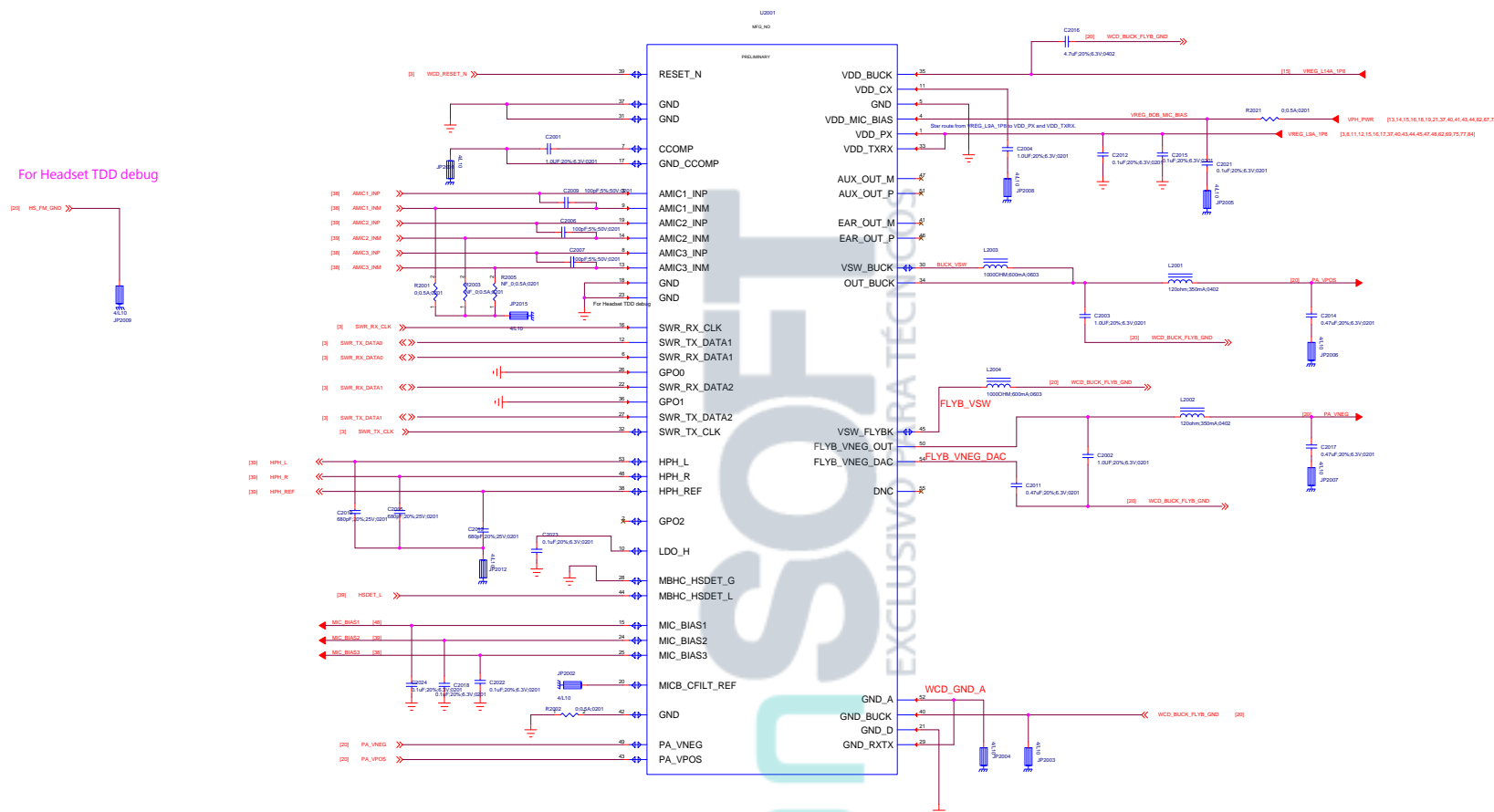
CAD NOTE:
Dedicated VIA to Main GND

NOTE:
BOOT_PWR net is 5VDC, cap is 0603. Do not use 0402 as may derate to -80%.

PMI632_Charger/PD PHY

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LTR	DESCRIPTION	DATE	APPROVE
A	INITIAL RELEASE		

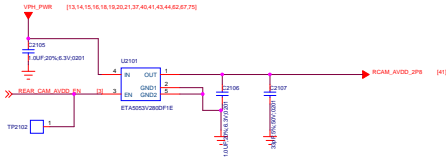
Title	Page Name = 20_WCD8370	REV: V10
DOCUMENT NO:	Design Name = 88718_1_13M14_20100	Sheet 15 of 15
DEPARTMENT:	DESIGNER/CAER = shangxi	
		
Date:	Page Modify Date = Wednesday, September 20, 2017	20 of 20



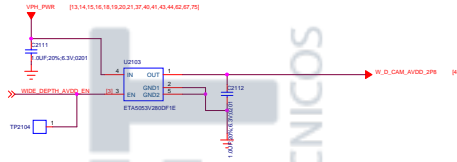
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REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE		

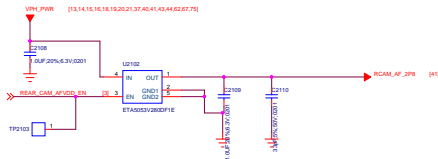
LDO for Rear&Front Camera AVDD 2.8V



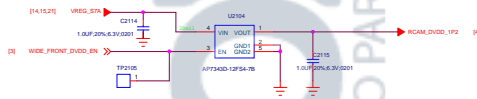
LDO for Depth AVDD 2.8V



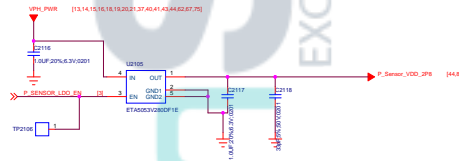
LDO for Rear Camera AFVDD 2.8V



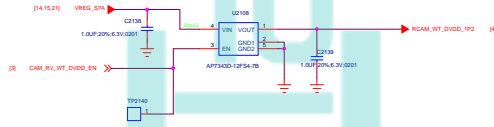
LDO for REAR DVDD 1.2V



LDO for Sensor 2.8V



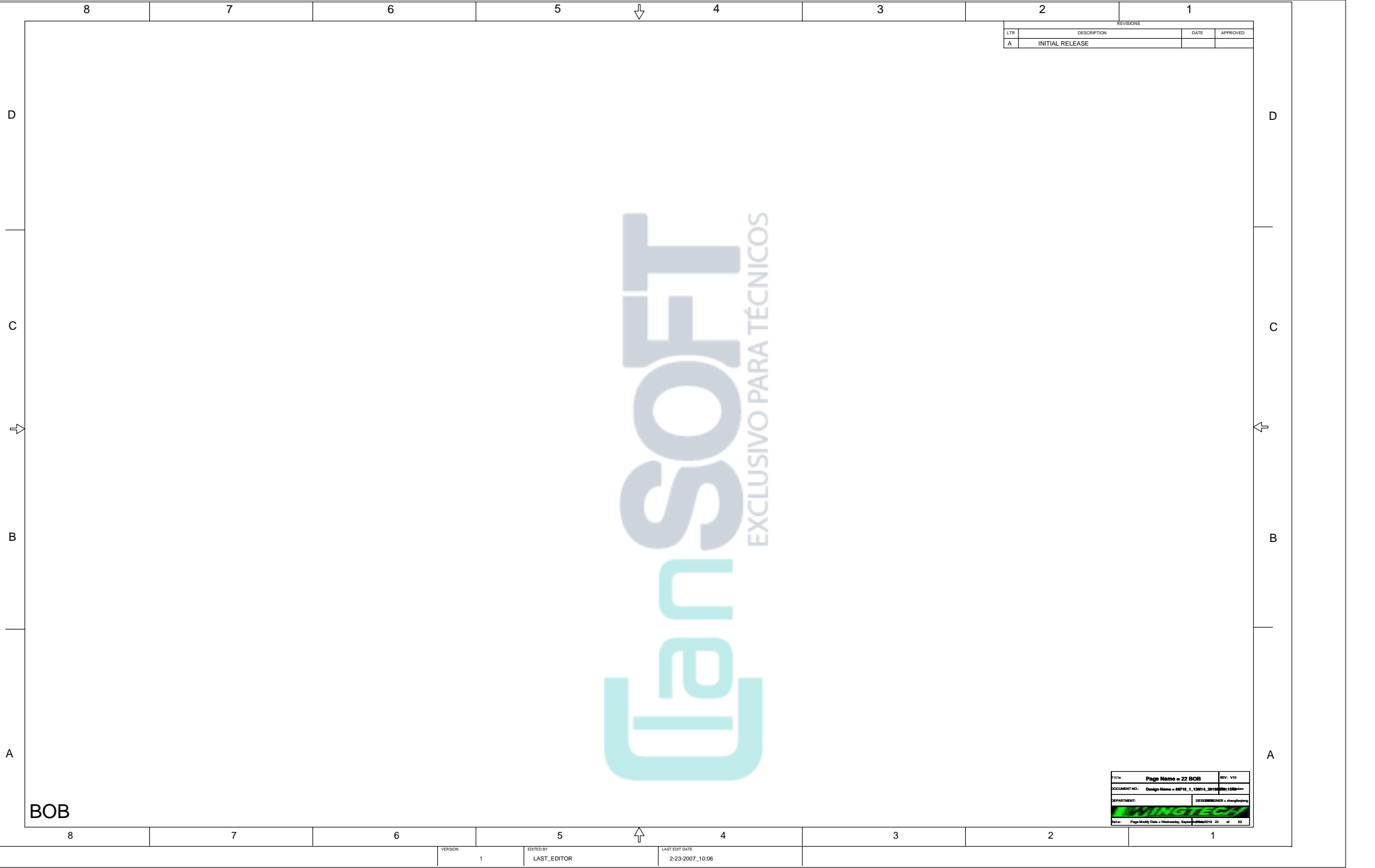
LDO for REAR W_T_M DVDD 1.2V



CAM eLDOs

File	Page Name = 21_CAM eLDO	Rev	V10
DOCUMENT NO.	Design Name = 88718_1_13814_30190	Rev	15
DEPARTMENT:	DESIGNER = chenghuijing		
Date:	Page Modify Date = Wednesday, 21	of	53

VERSION	EDITED BY	LAST EDIT DATE
1	LAST_EDITOR	2-23-2007_10:06



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE		

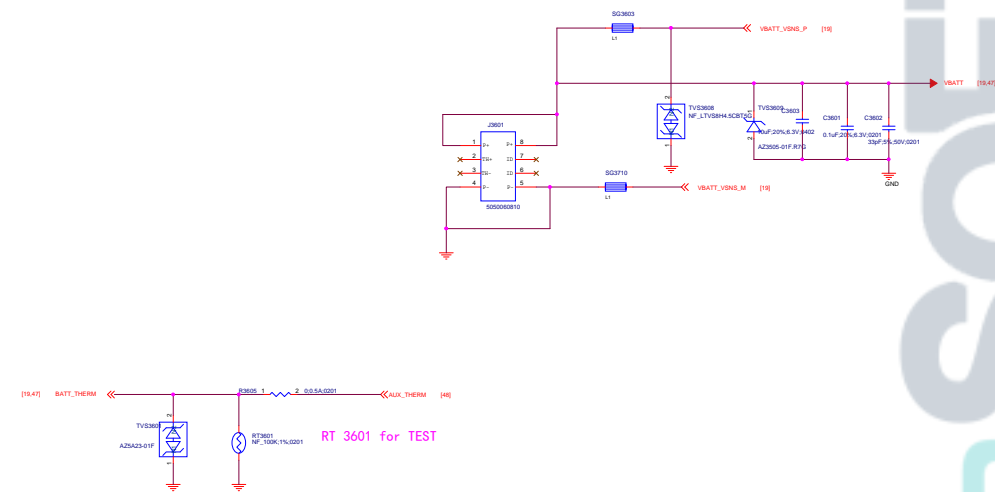
1114	Page Name = 22 BOB	REV: 1/10
DOCUMENT NO:	Design Name = 80714_1_13M14_2010	Rev: 1300000
DEPARTMENT:	DESIGN/ENGINEERING - PLANT/WORKSHOP	
Rev:	Page Monthly Date = Wednesday, 20/06/2010 10:06	Rev: 1300000

VERSION	EDITED BY	LAST EDIT DATE
1	LAST_EDITOR	2-23-2007_10:06

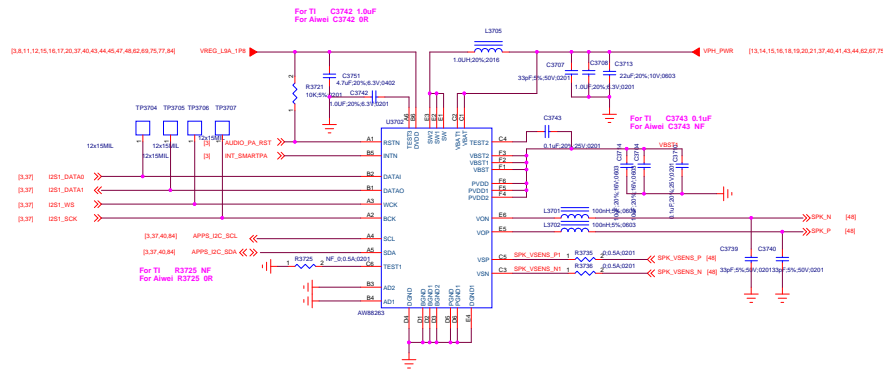


Title		32.CODEC_Cirrus	REV: V10
DOCUMENT NO:		88718_1_13814_20180808_1542	Rev: 0
DEPARTMENT:		DEPARTMENT	DESIGNER: DESIGNER
Date:		Wednesday, September 04, 2019	Sheet 32 of 65

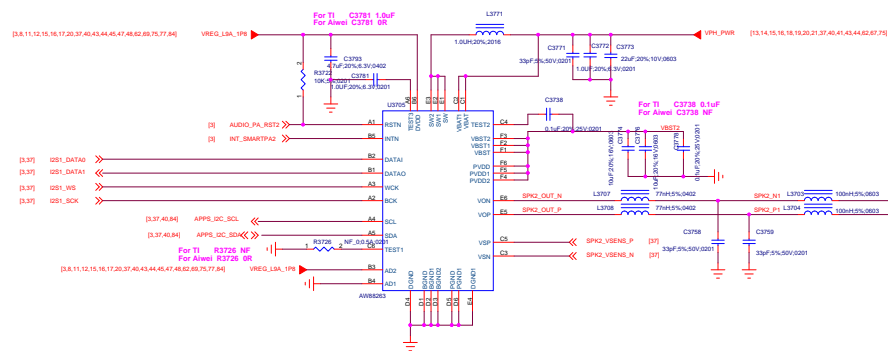
BATTERY CONNECTOR



SPK

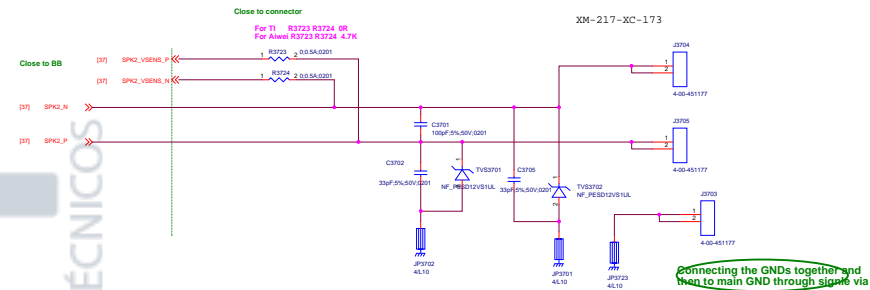


```
SMART PA/CIRRUSLOGIC/CS35L41/I2C Address Write 0X80 Read 0x81 AD1=0 AD0=0
```



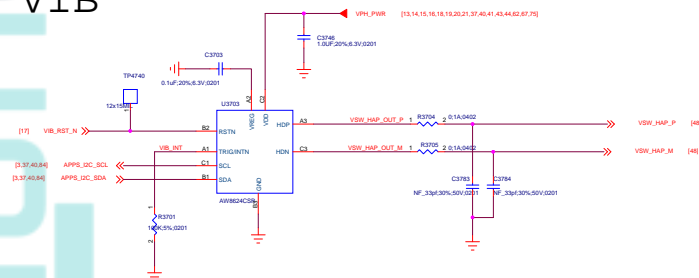
SMART PA/CIRRUSLOGIC/CS35L41/I2C Address Write 0X82 Read 0x83 AD1=0 AD0=1

SPK2&Receiver



Connecting the GNDs together and then to main GND through single via

VIB



[48] AMIC1_INP_CON >> 1 2 0.1A:0402 AMIC1_INP [20]

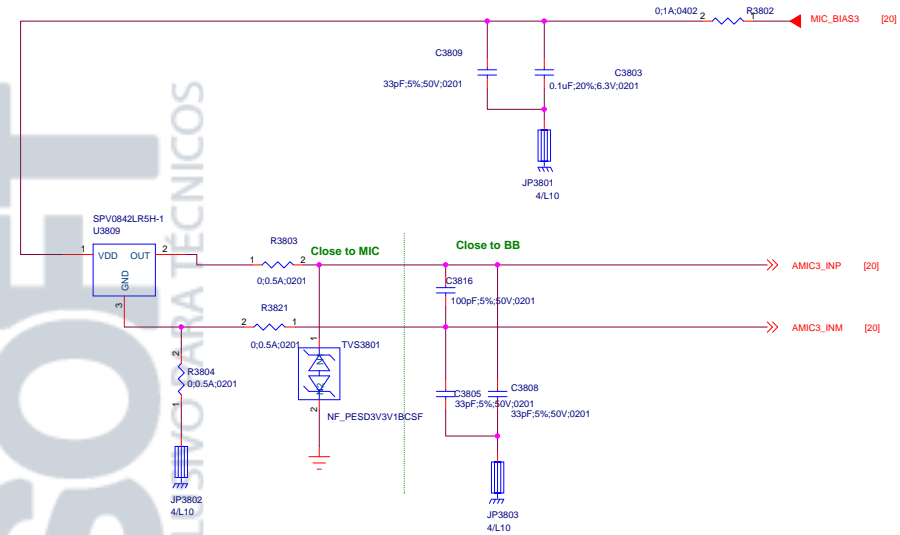
R3807

[48] AMIC1_INM_CON >> 1 2 0.1A:0402 AMIC1_INM [20]


C3802 68pF:5%:50V:0201

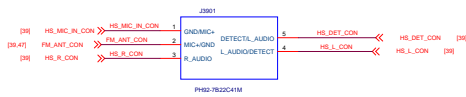
C3811 68pF:5%:50V:0201

JP3806 4/L10

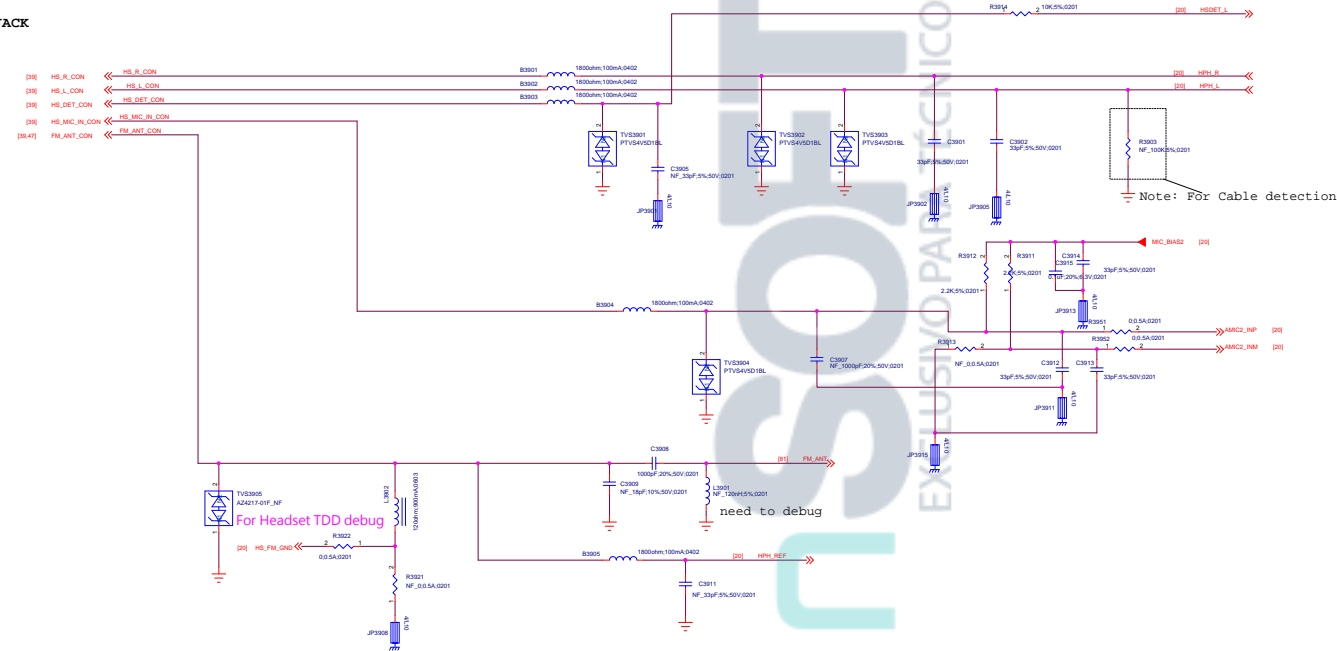


Note 63-1: 1 uF for ACC mode

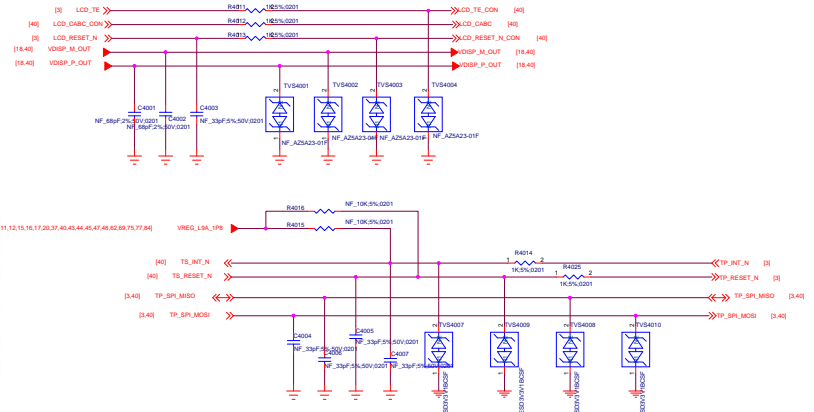
Title	Page Name = 38_MIC		REV: V10
DOCUMENT NO.:	Design Name = 88718_1_13M14_20190901		1542
DEPARTMENT:	DESIGNER = zhangfengqiang		
			
Date:	Page Modify Date = Wednesday, September 18, 2019 38 of 53		



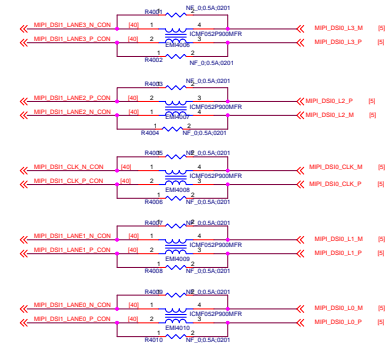
AUDIO JACK



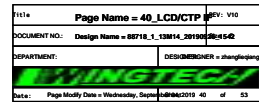
EXCLUSIVO PARA TÉCNICOS



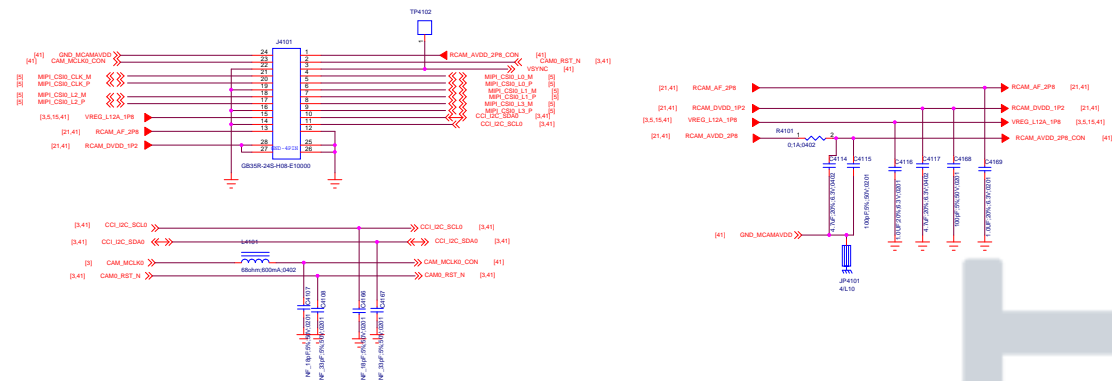
EXCLUSIVO PARA TÉCNICOS



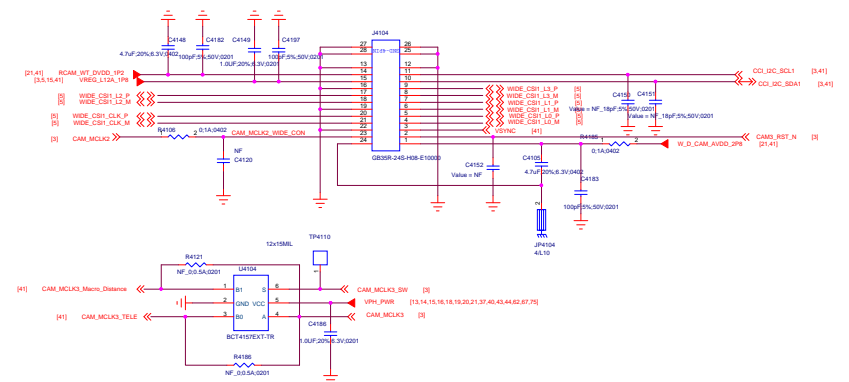
EXCLUSIVO PARA TÉCNICOS



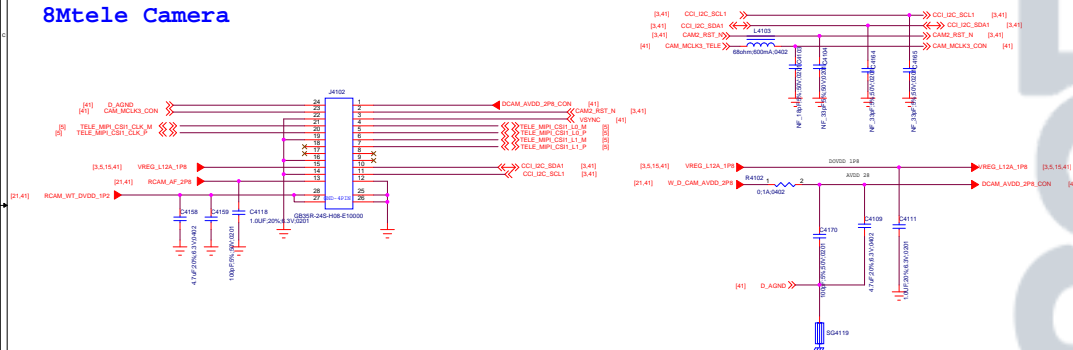
Main Camera 16M



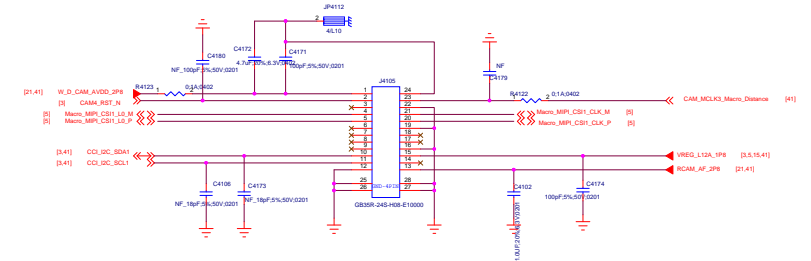
Wide Camera 8M



8Mtele Camera

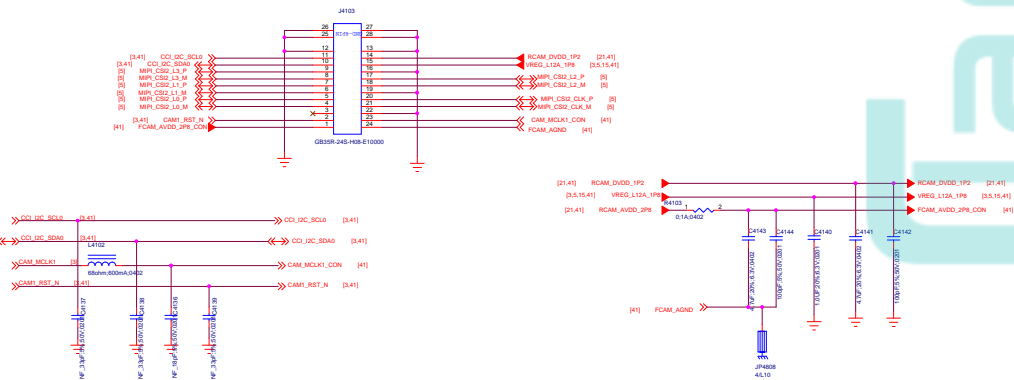


Macro distance Camera

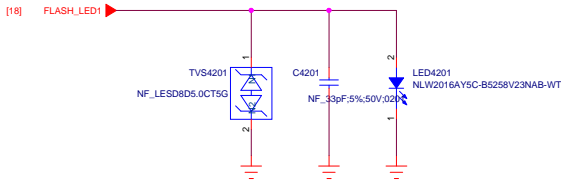


Front Camera

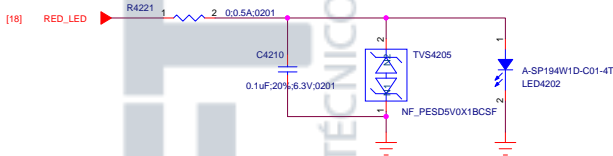
Front Camera 16M



FLASH_DRIVER

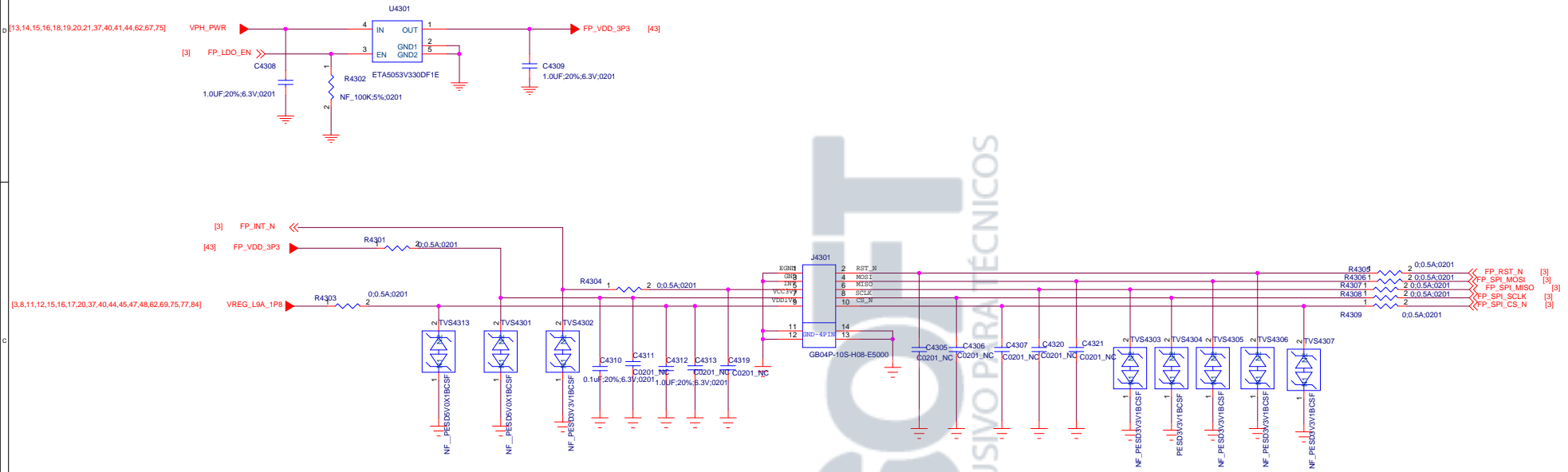


LED_DRIVER



TOF

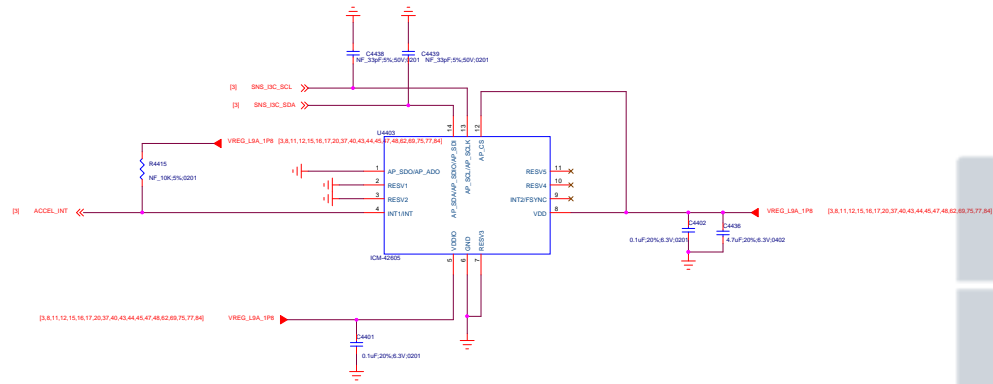
FP LDO 3.3V



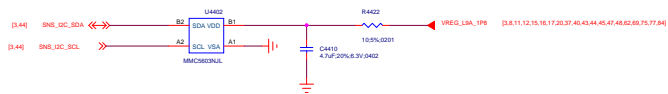
Fingerprint

ACCELEROMETER

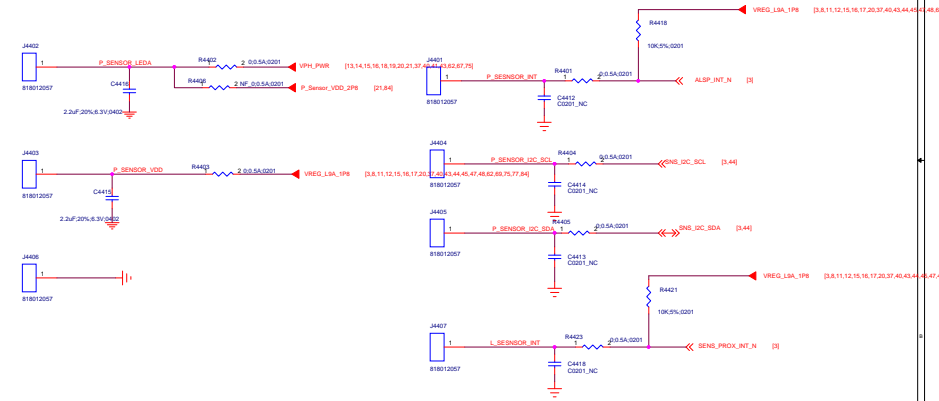
A+G SENSOR



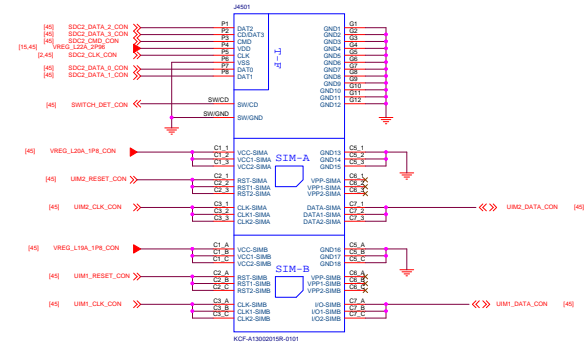
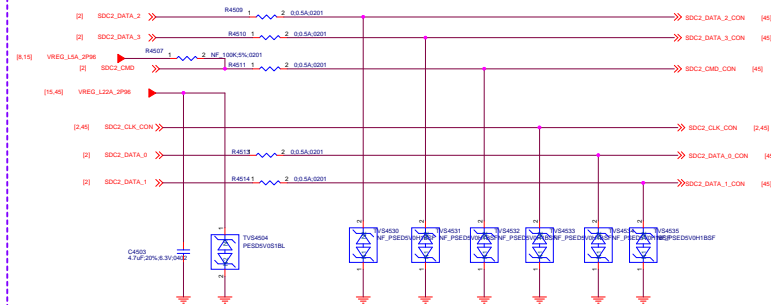
Magnetic Sensor



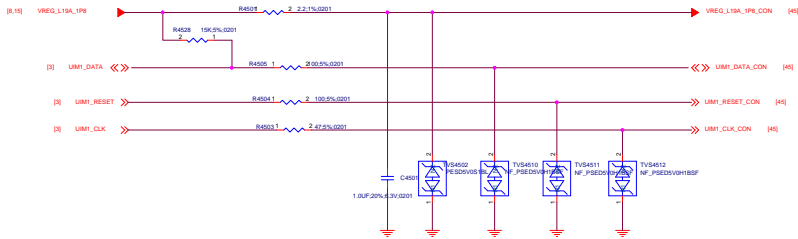
ALP+P SENSOR



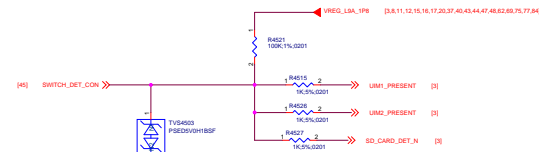
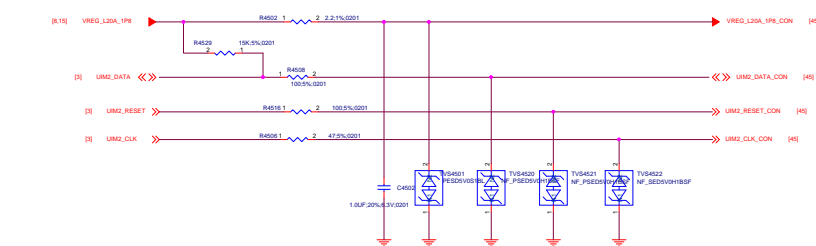
TF CARD



USIM1

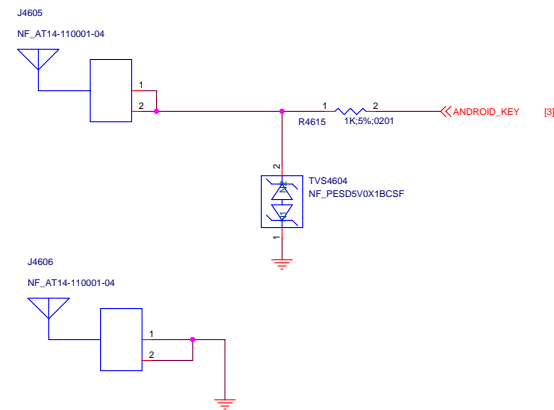
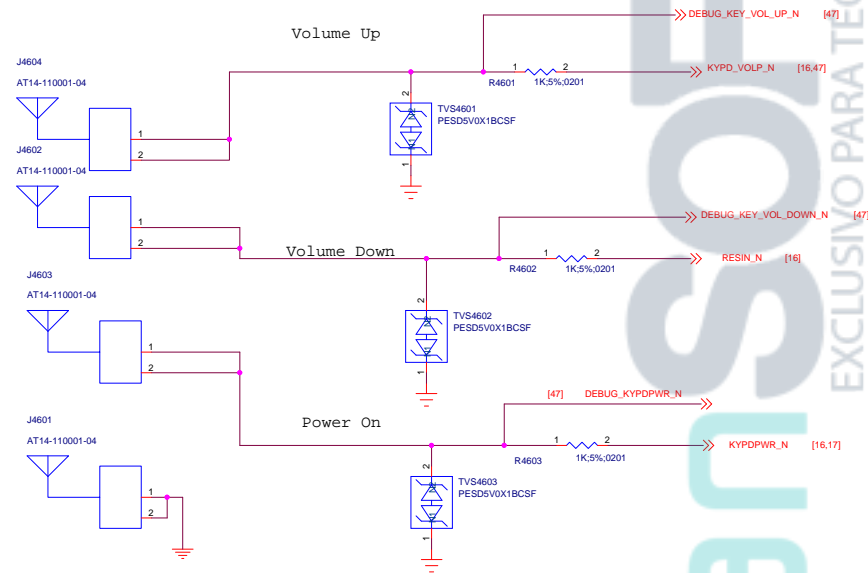


USIM2



Symbol	Value	Unit
R4509	10K	Ω
R4510	10K	Ω
R4511	10K	Ω
R4512	10K	Ω
R4513	10K	Ω
R4514	10K	Ω

Keys

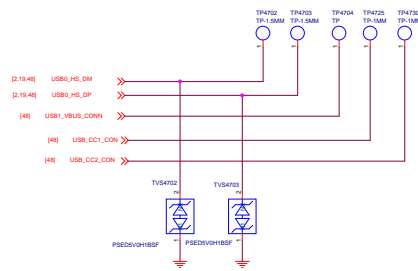


Schematic design notice of "75_PERI_KEYPAD" page.

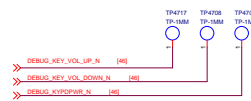
Note 75-1: DO NOT put pull-up resistor on PWRKEY

Note 75-2: Volume Up : HOME Key / GND
Volume Down : KPROW/KPCOLO

USB

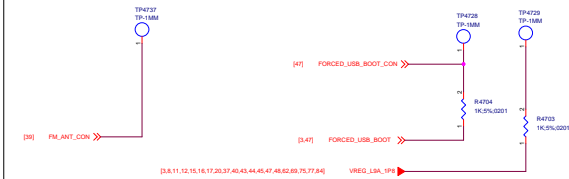


KEYS

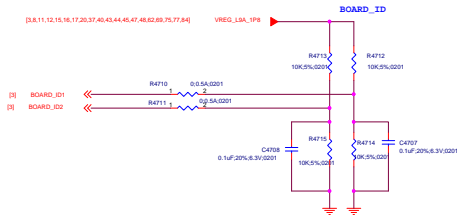


DTV test

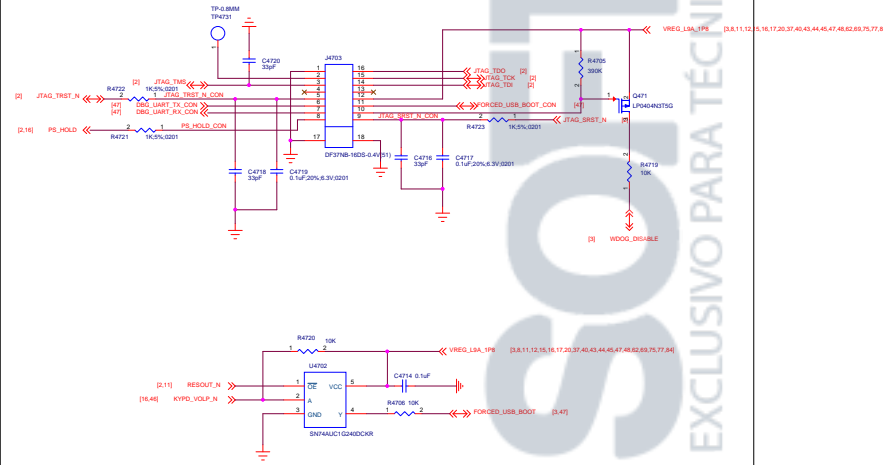
TEST



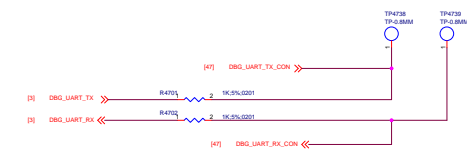
BOARD ID



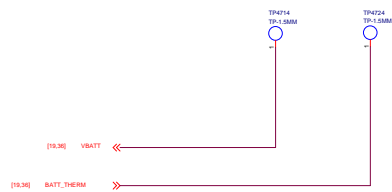
JTAG CONNECTOR



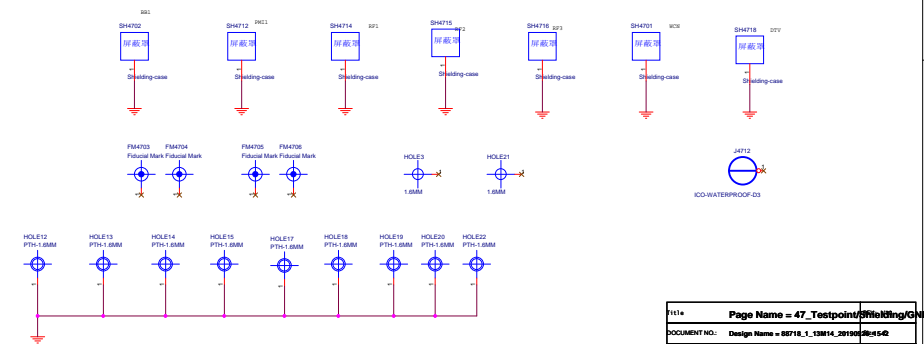
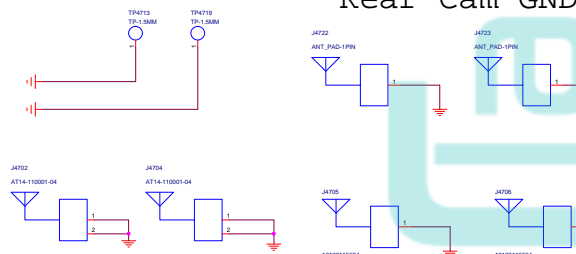
UART



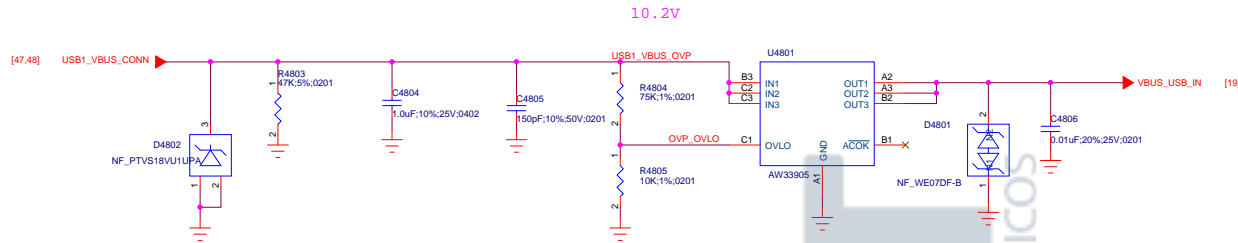
BATTERY



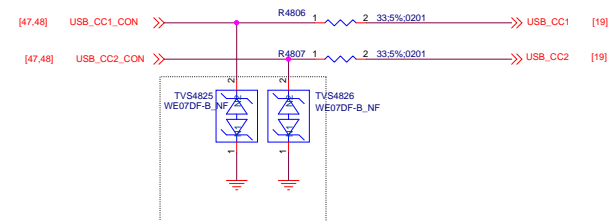
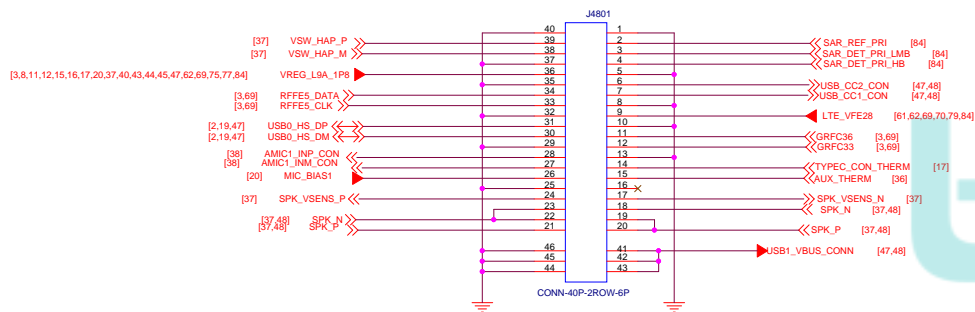
GND

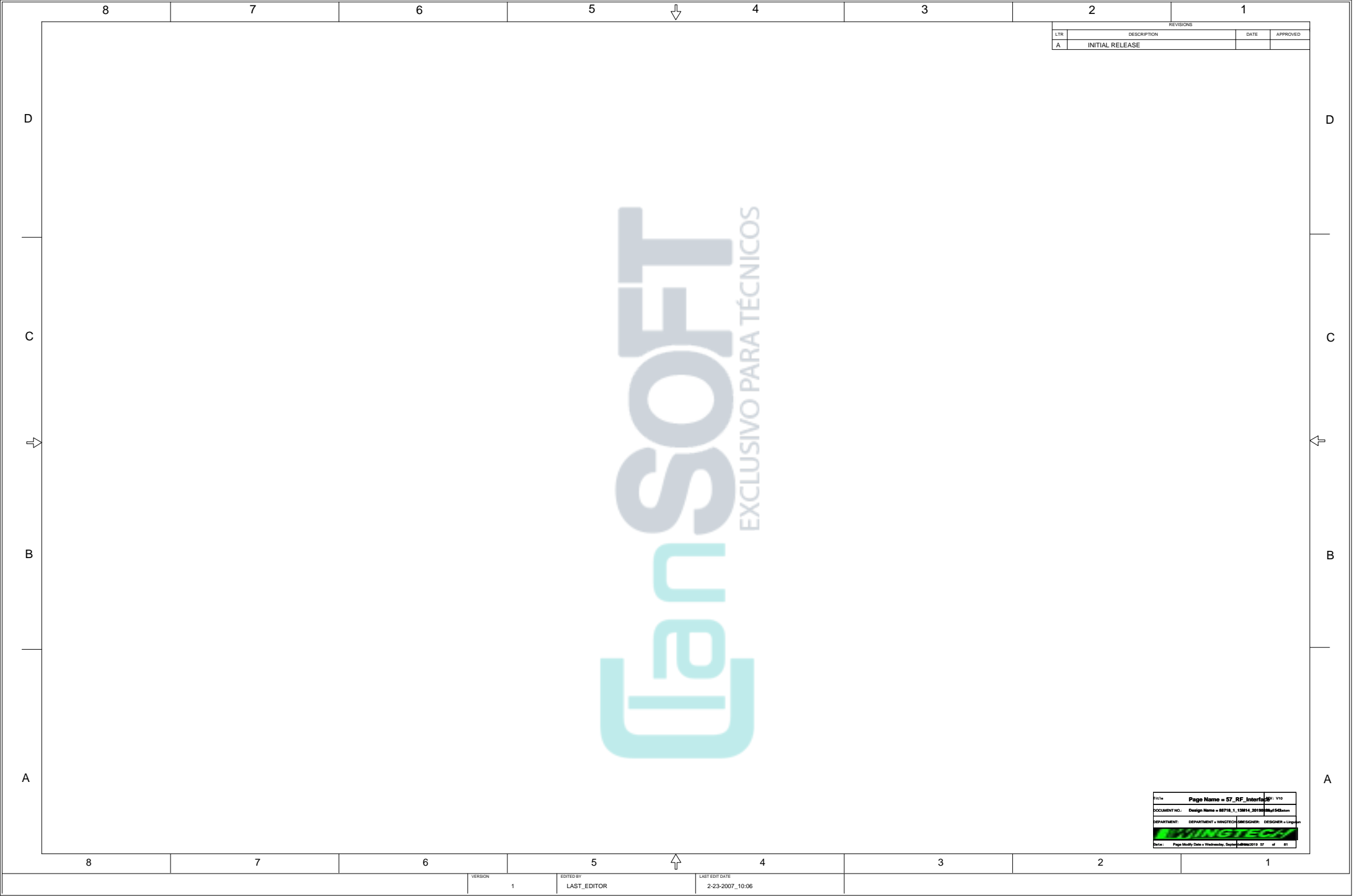


OVP



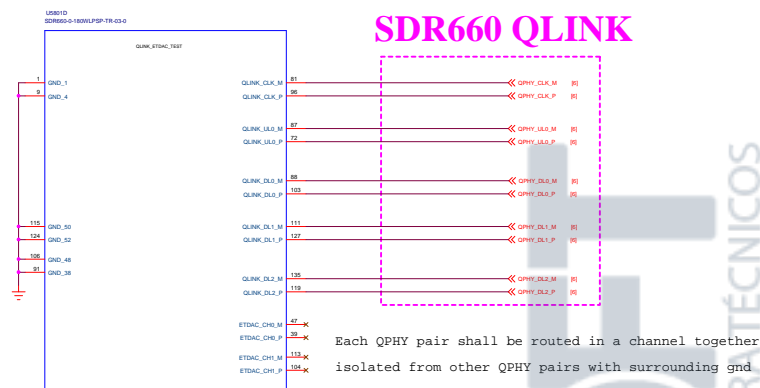
Sub Board Connector



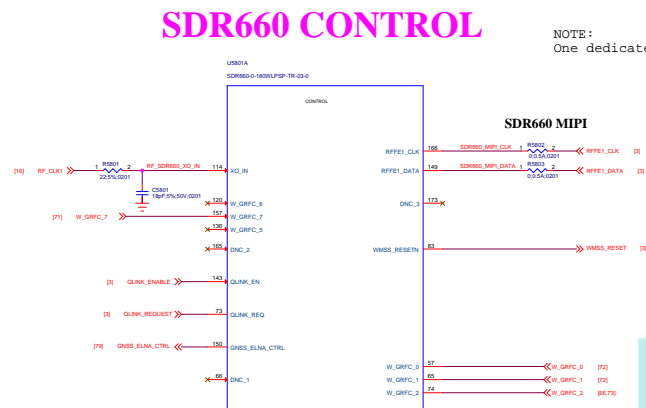


SDR660 MSS &GND

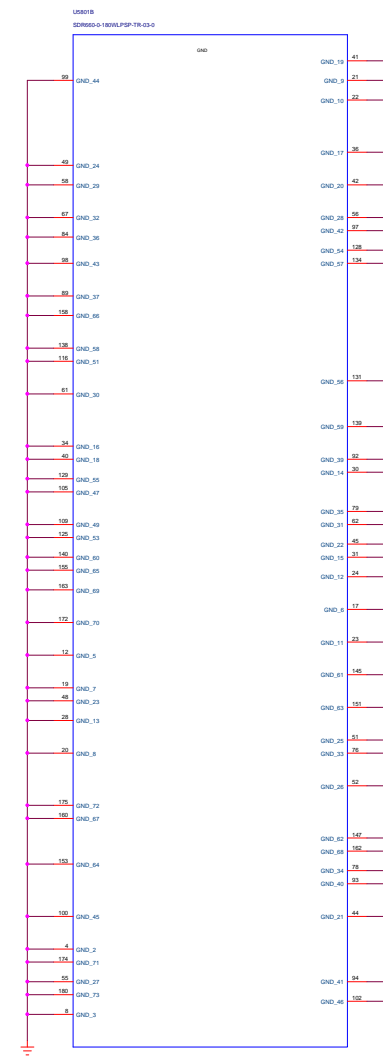
REVISIONS		DATE	APPROVE
A	INITIAL RELEASE		



Each QPHY pair shall be routed in a channel together
isolated from other QPHY pairs with surrounding gnd

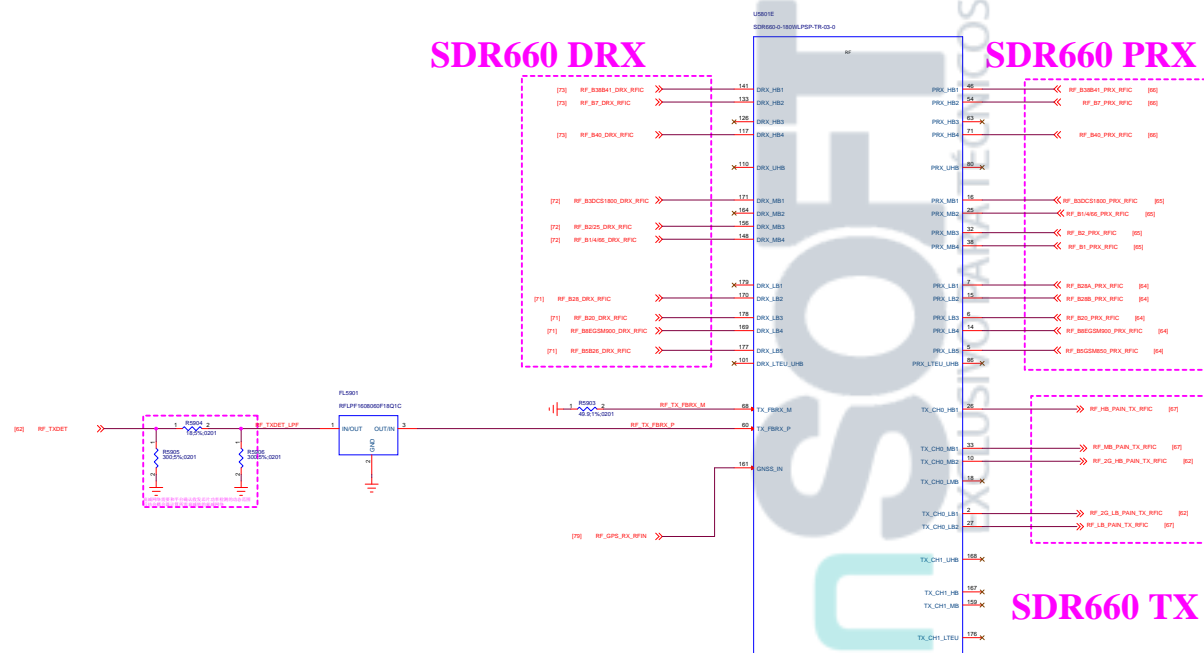


NOTE:
One dedicated RFFE bus is required for SDR660 debug purposes



Title	Page Name = 58_Transceiver_MSS_G	
DOCUMENT NO:	Design Name = 88718_1_13M14_20190525_50item	
DEPARTMENT:	DEPARTMENT = VINGTECH	DRAWN: DESIGNER = Lin
AVINGTECH		
Date:	Page Modify Date = Wednesday, September 26, 2012 58 of 81	

SDR660 Tx,PRX,DRX,FBRX



WCDMA

B1 (2100)
B2 (1900)
B4 (1700/2100)
B5 (850)
B8 (900)

GSM

B2 (1900)
B3 (1800)
B5 (850)
B8 (900)

CDMA

BC0 (850)
BC1 (1900)
BC10 (850+)

2ULCA CA_41C

LTE

B1 (2100)
B2 (1900)
B3 (1800)
B4 (1700/2100)
B5 (850)
B7 (2600)
B8 (900) (AT&T)
B12 (lower 700 abc)
B13 (upper 700)
B14 (AT&T)
B17 (lower 700 bc)
B20
B25 (1900+) (Sprint)
B26 (850+) (Sprint)
B29 (AT&T)
B30
B38 (TD2600)
B39
B40
B41 (TD2500)
B41 HPAUE (TD2500) (Sprint)
B66 (AWS1-4)
B71 (600 US) (T-mobile)

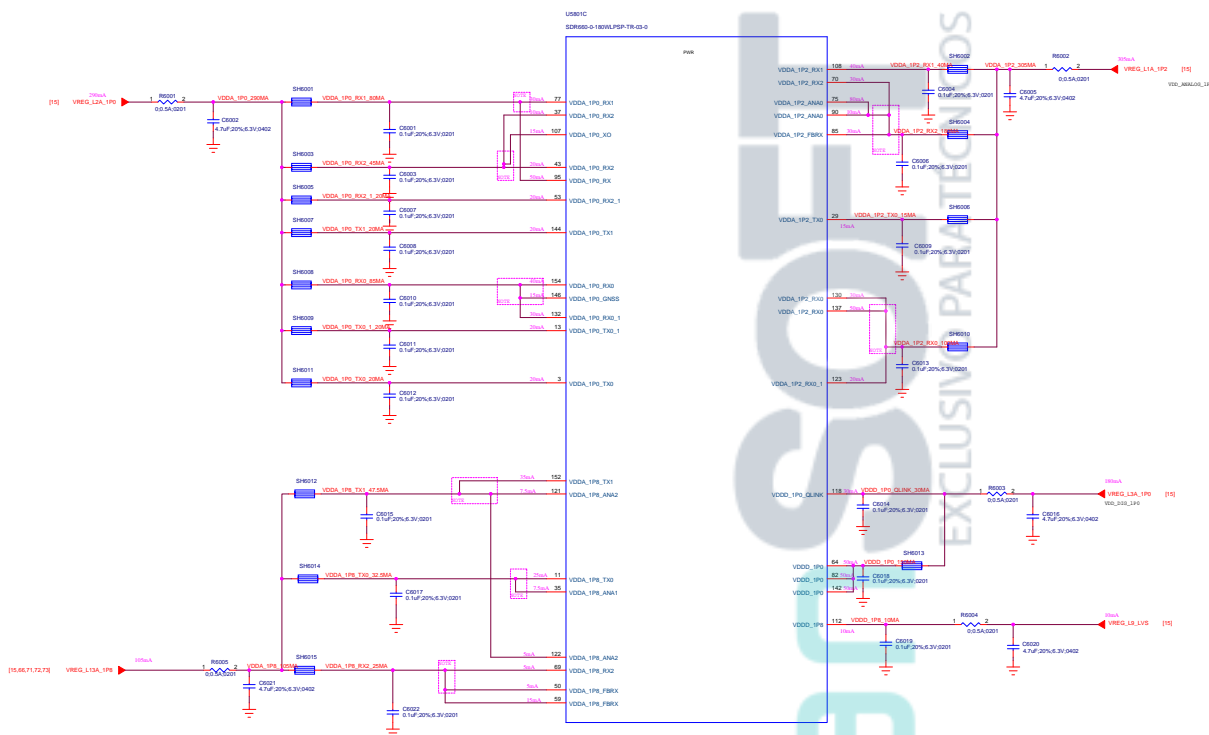
2DLCA

2A-4A
2A-5A
2A-7A
2A-12A
2A-13A
2A-14A
2A-29A
2A-30A
2A-71A
4A-5A
4A-12A
4A-13A
4A-29A
4A-30A
4A-71A
5A-30A
5A-66A
12A-30A
12A-66A
13A-66A
14A-30A
14A-66A
25A-26A
29A-30A
29A-66A
30A-66A
66A-71A
4A-7A
7A-12A
2A-17A
4A-17A
5A-7A
7A-66A

- DA outputs have no DC bias and they are DC grounded on chip.
- If following component (switch/PA) requires non-zero DC, then a series DC blocking cap is needed
- NC for unused LNA and DA Port

SDR660 POWER

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE		

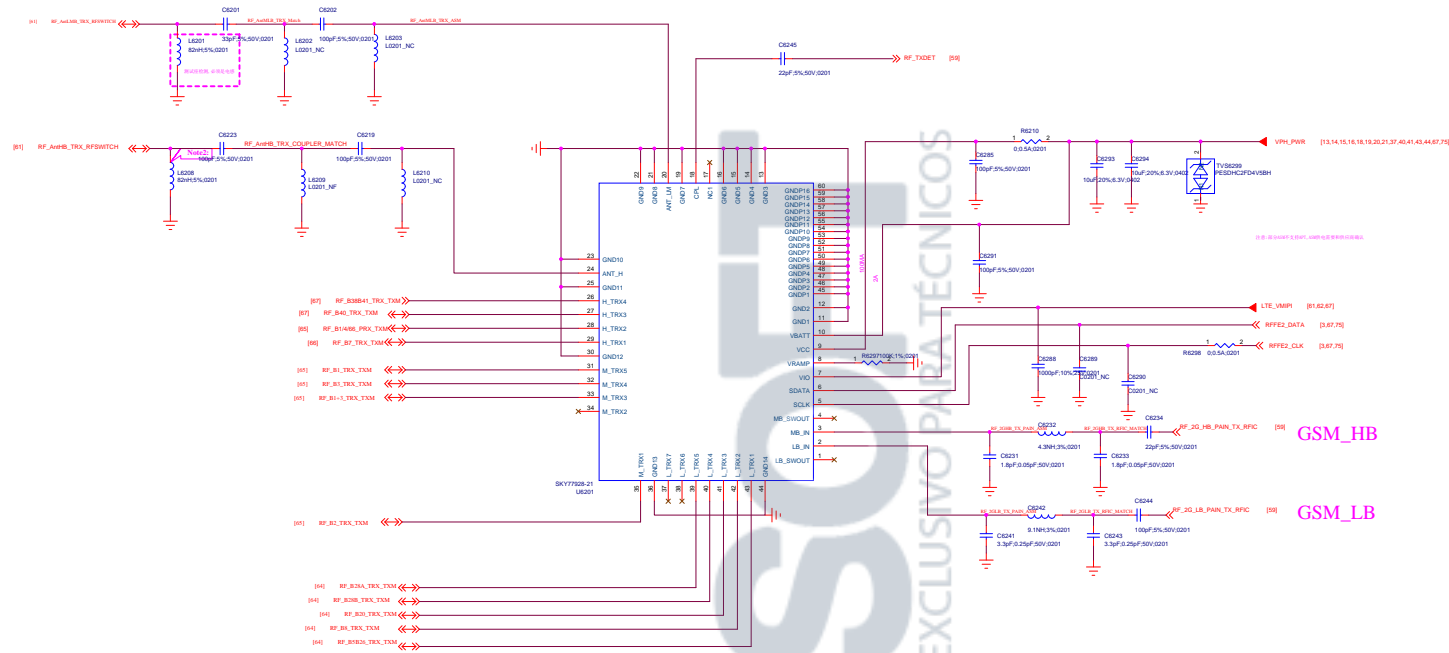


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DOCUMENT NO.	Design Name = 88718_1_13M14_20150901
DEPARTMENT	DEPARTMENT = WINTECH
DESIGNER	DESIGNER = Ling
DATE	Page Modify Date = Wednesday, 2015/09/01 15:05

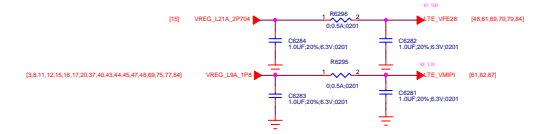
VERSION	1
EDITED BY	LAST_EDITOR
LAST EDIT DATE	2-23-2007_10:06

Note2: MUST BE IND FOR RF SWITCH DETECT

ASM_LMB



POWER SUPPLY

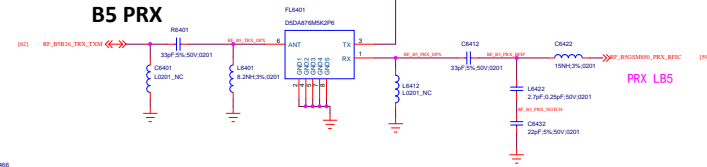


Note1: MXD8641 V1 CAN GROUD CONFIRMED WITH FAE

Note2: MUST BE IND FOR RF SWITCH DETECT

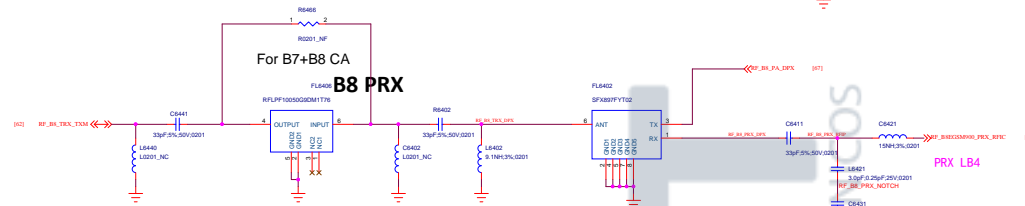
Super ROW: B26 DPX
Brazil&Latam: B5 DPX

B5 PRX



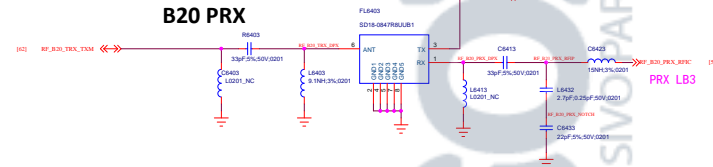
For B7+B8 CA

B8 PRX



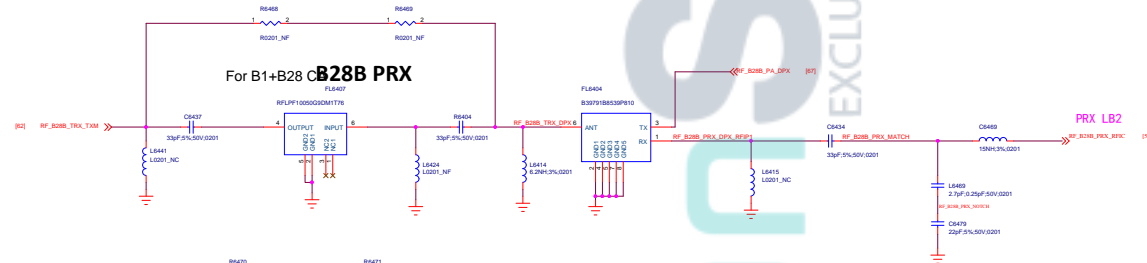
Super ROW: B20 DPX
Brazil&Latam: B12 DPX

B20 PRX



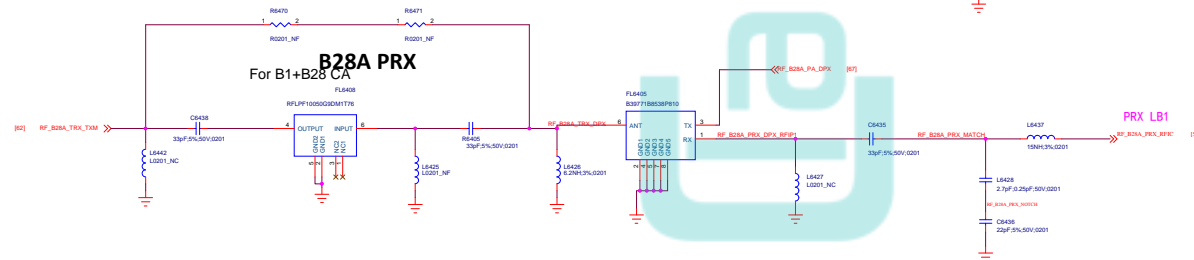
For B1+B28 CB28B PRX

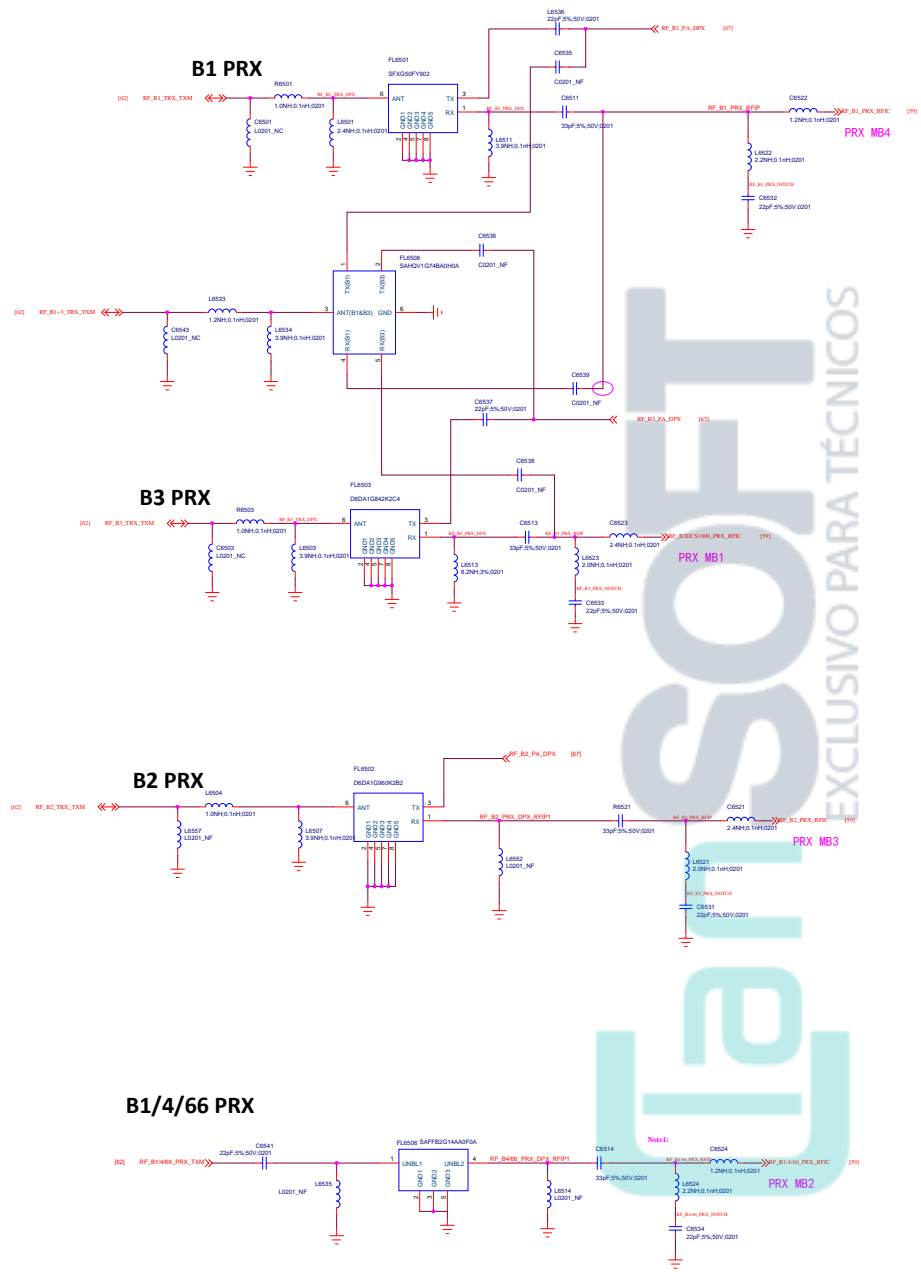
B28B PRX



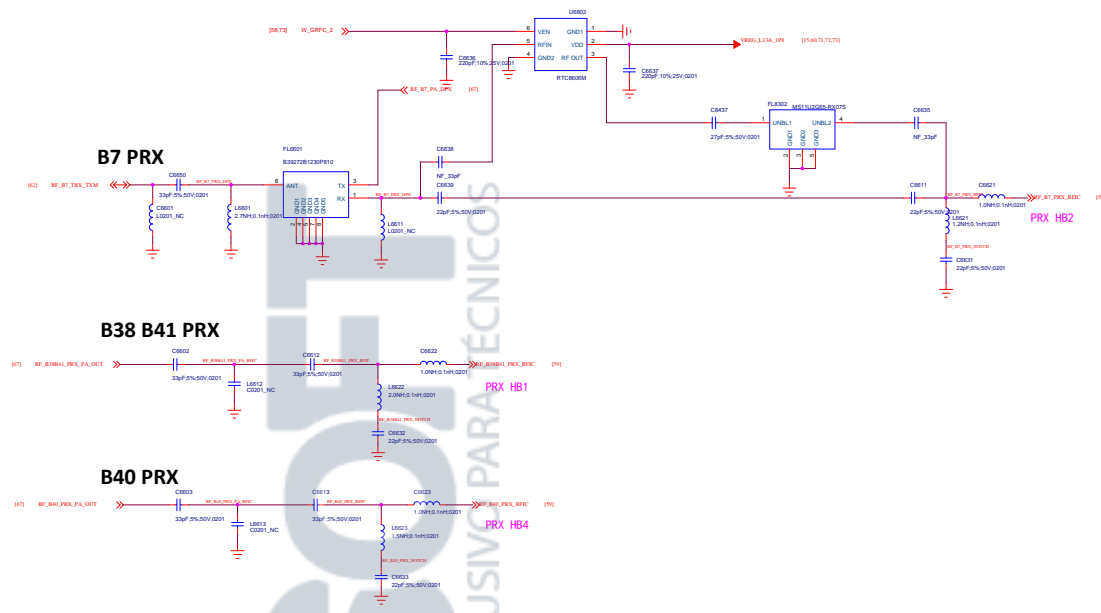
For B1+B28 CA

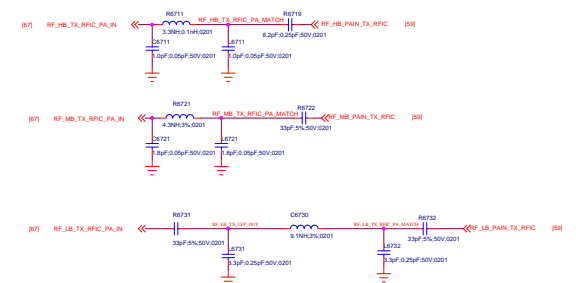
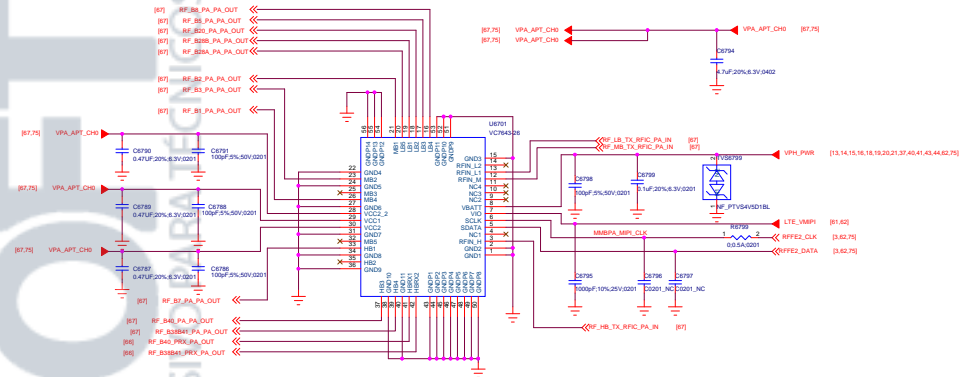
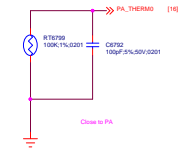
B28A PRX

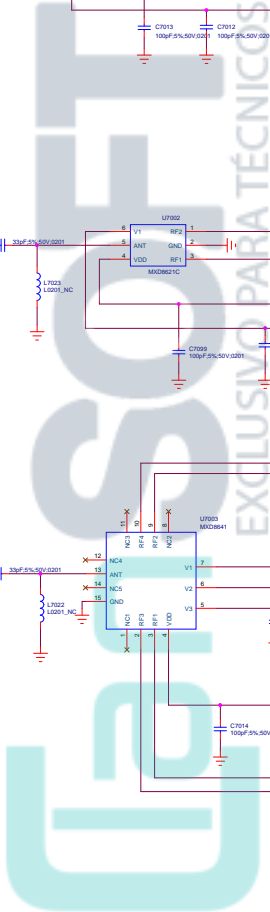


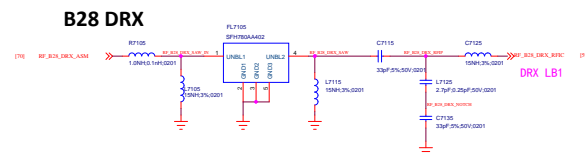
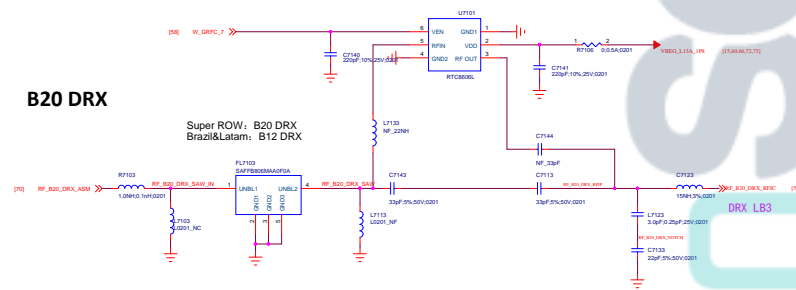
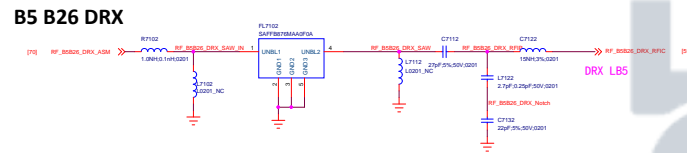
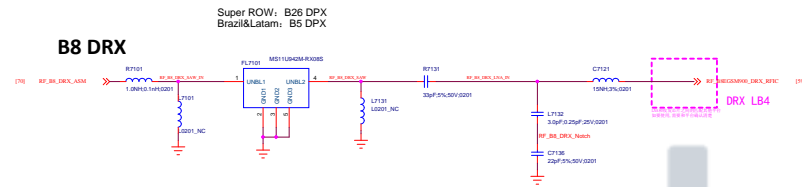


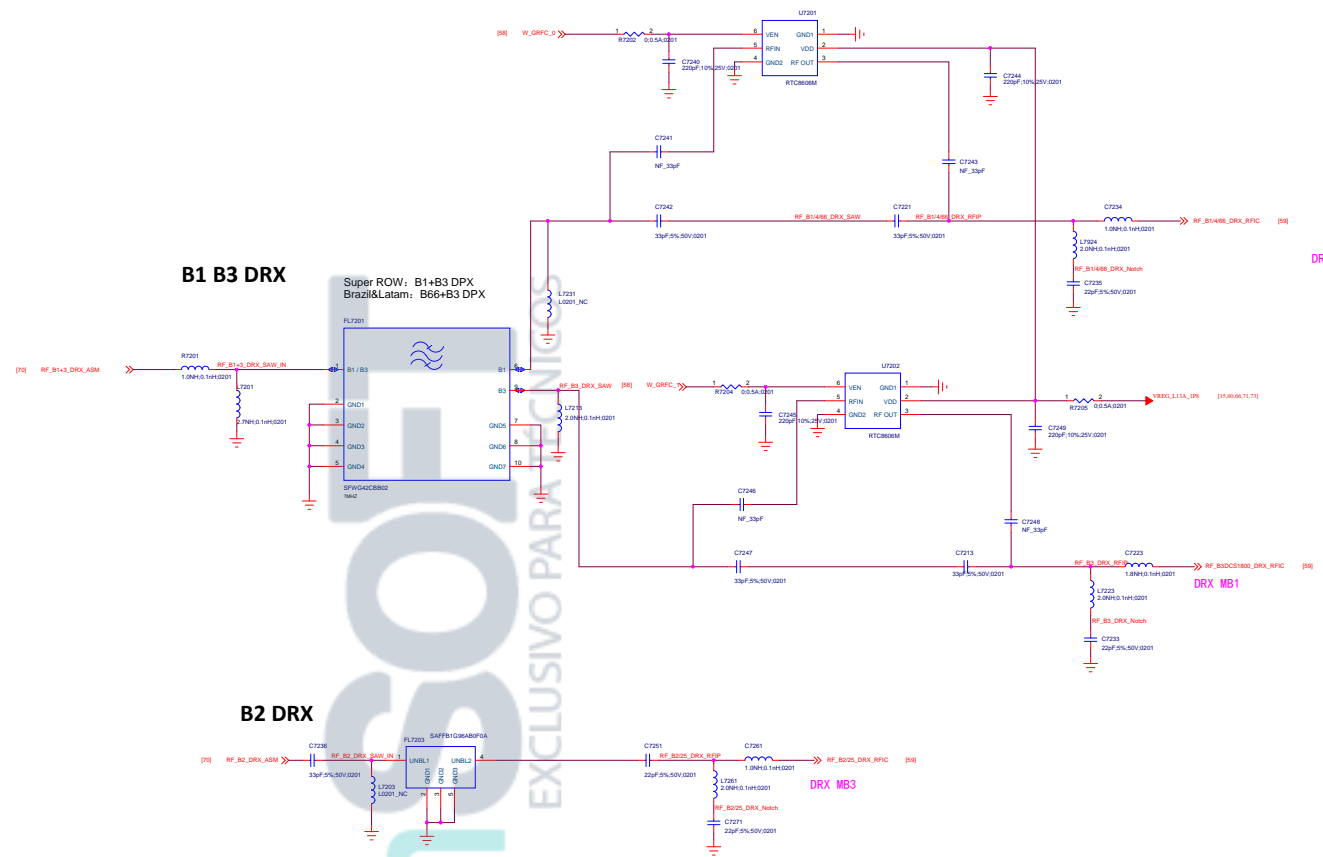
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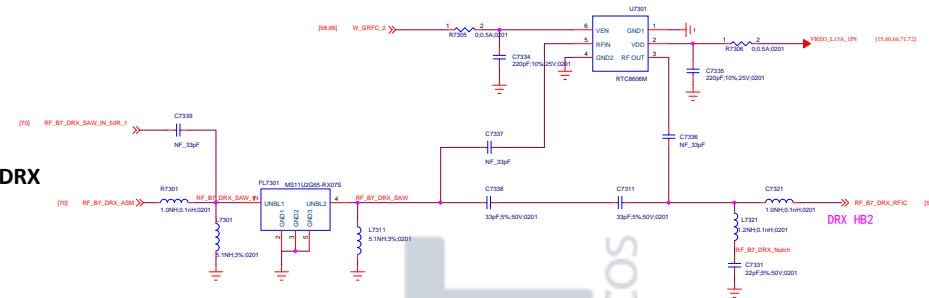




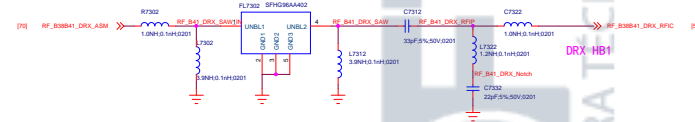




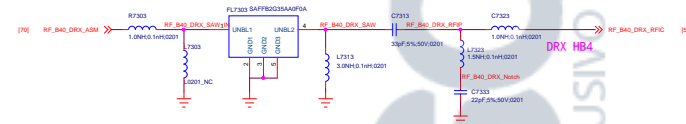
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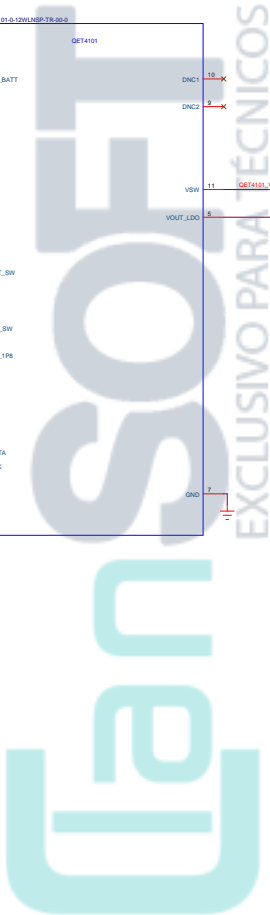


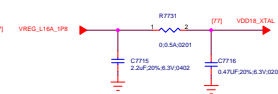
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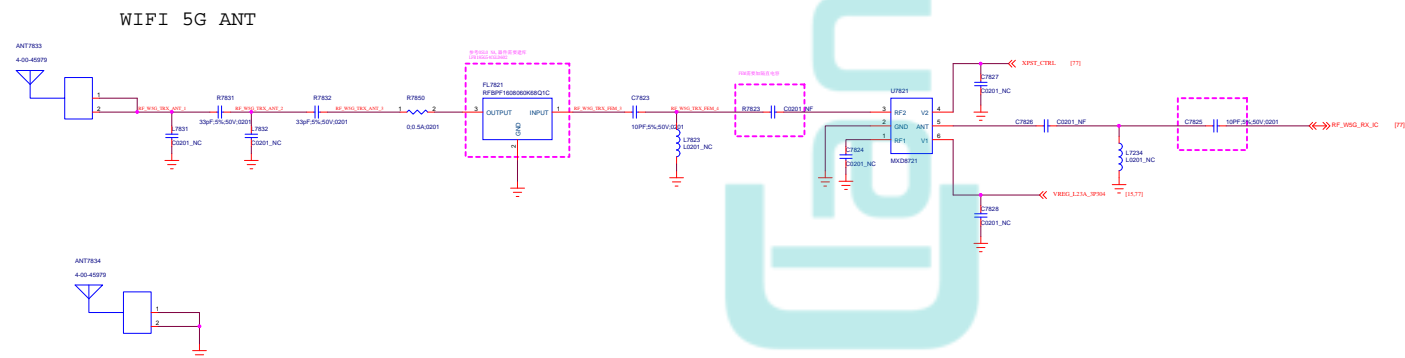
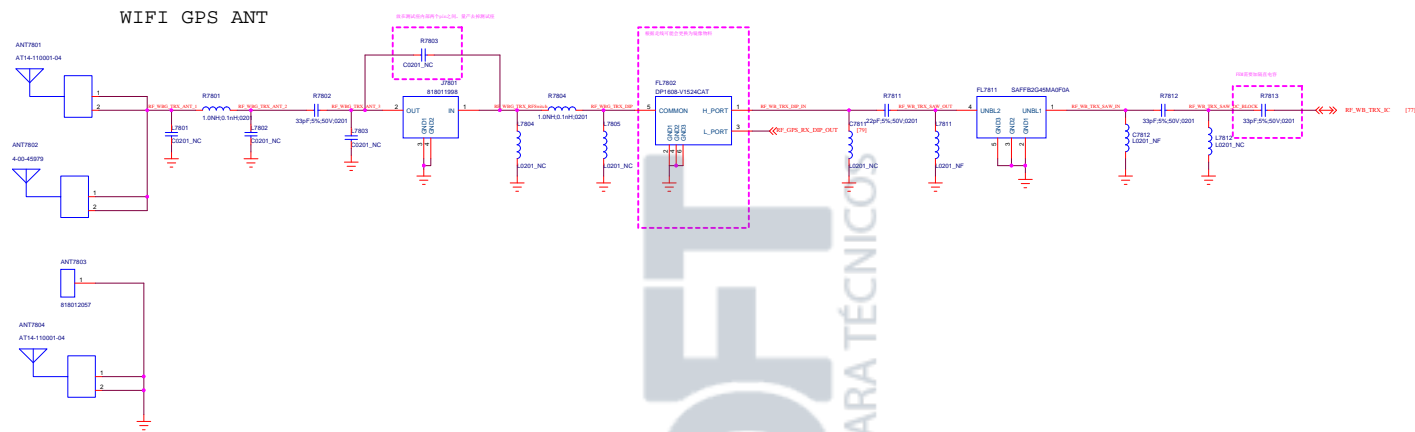


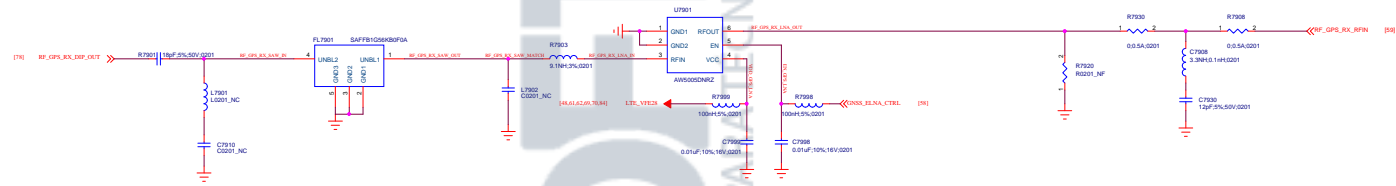
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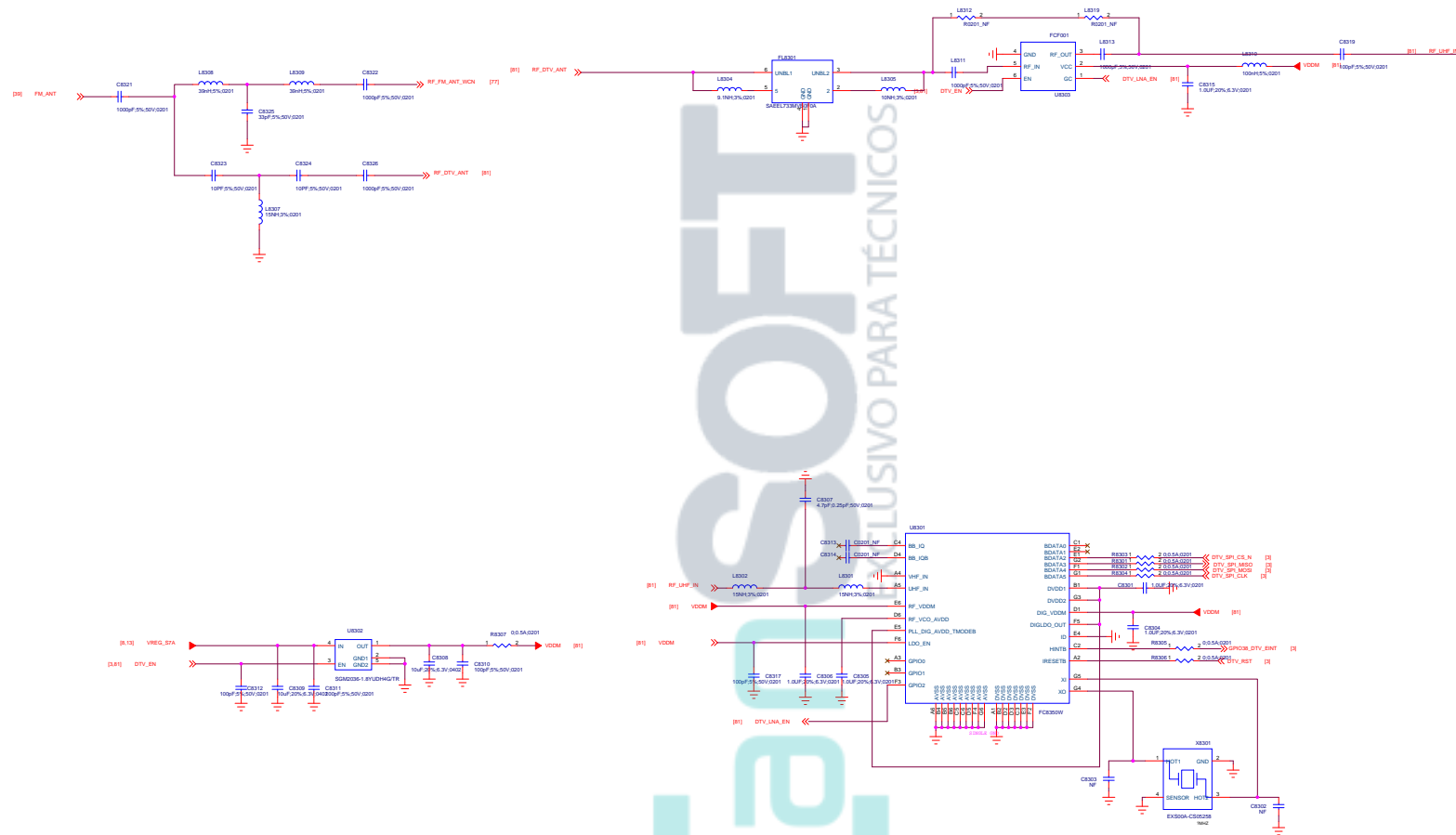








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